RAiO

RA8860

80x2 dots 16-Colors

LCD Driver

Specification

Version 1.3

August 8, 2013

RAiO Technology Inc.

Update History		
Version	**Date**	**Description**
1.0	May 4, 2010	Preliminary version
1.1	September 28, 2010	1. Add Chapter 2 - Available package type 2. Add Figure 3-3、Table 3-1、Figure 3-4 3. Add Table 7-6 4. Update Figure 8-1、Figure 8-2、Figure 8-3
1.2	March 15, 2011	1. Add Figure 7-9 2. Insert Chapter 9 -Register Setting Sequence 3. Update Chapter 10 -Demo Program (LCD_Initial())
1.3	May 31,2011	1. Update Table 6-1、Table 7-4
	August 8, 2013	1. Add Note on Figure 3-2

Chapter Contents Page

1. Overview

The RA8860 is a LCD Driver & Controller for Field Sequential Liquid Crystal Display (FSLCD) systems. It contains 80 segment and 2 common driver circuits. This chip is connected directly to a MCU, support 3-wire, 4-wire serial peripheral interface (SPI) and I^2C interface, display data can stores in an on-chip display data RAM of 640bits. It performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, it also can produce LED driving signals to generate RGB LED backlight system if necessary.

2. Features

- 80SEGx 2COM Drive Outputs
- Supports Serial I^2C, 3/4-wires MCU Interface
- Supports 8 or 16 Colors Display
- Build-in 640-bits Display RAM
- Duty : Static, 1/2 Duty
- Build-in Voltage Booster(4X) and Voltage Follower for LCD Driver
- Supports Blinking Mode
- Build-in RGB LED Driver for LED and Max. 80mA Sink Current for each Driver
- Build-in RC Oscillator
- Supports Multi FSLCD Drivers (Master / Slave Mode)
- Available package type: LQFP-128pin, Bare die
- Supply Voltage : 2.7~5.5V

3. Pin Configuration

3-1 Block Diagram

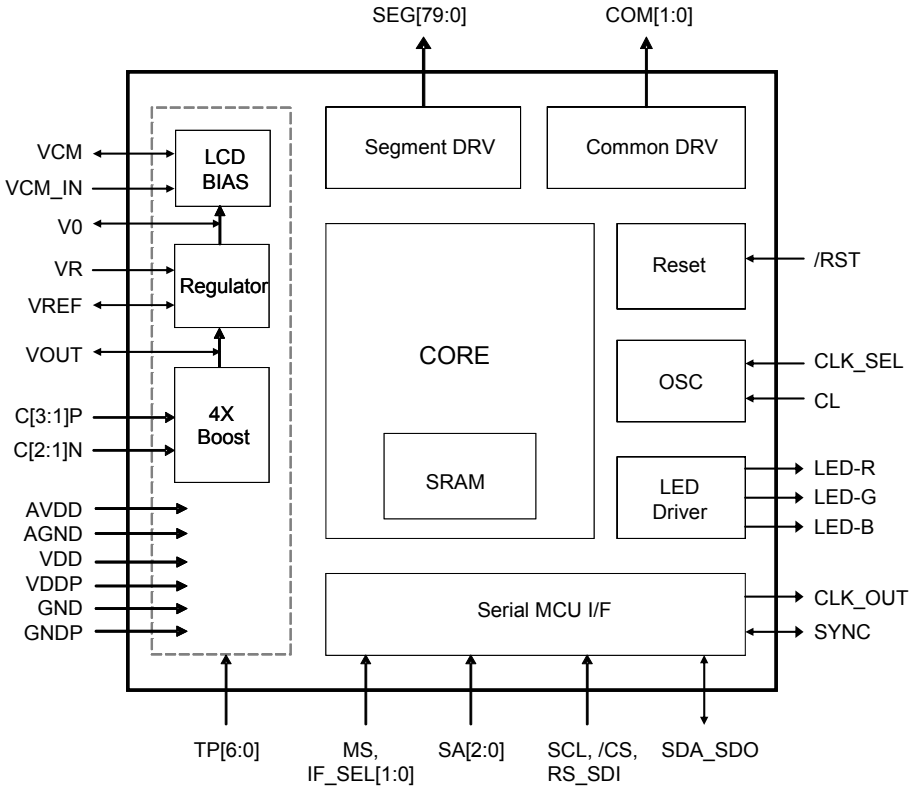


Figure 3-1 : RA8860 Block Diagram

3-2 PAD Diagram

Note : Please connect the substrate to GND or floating.

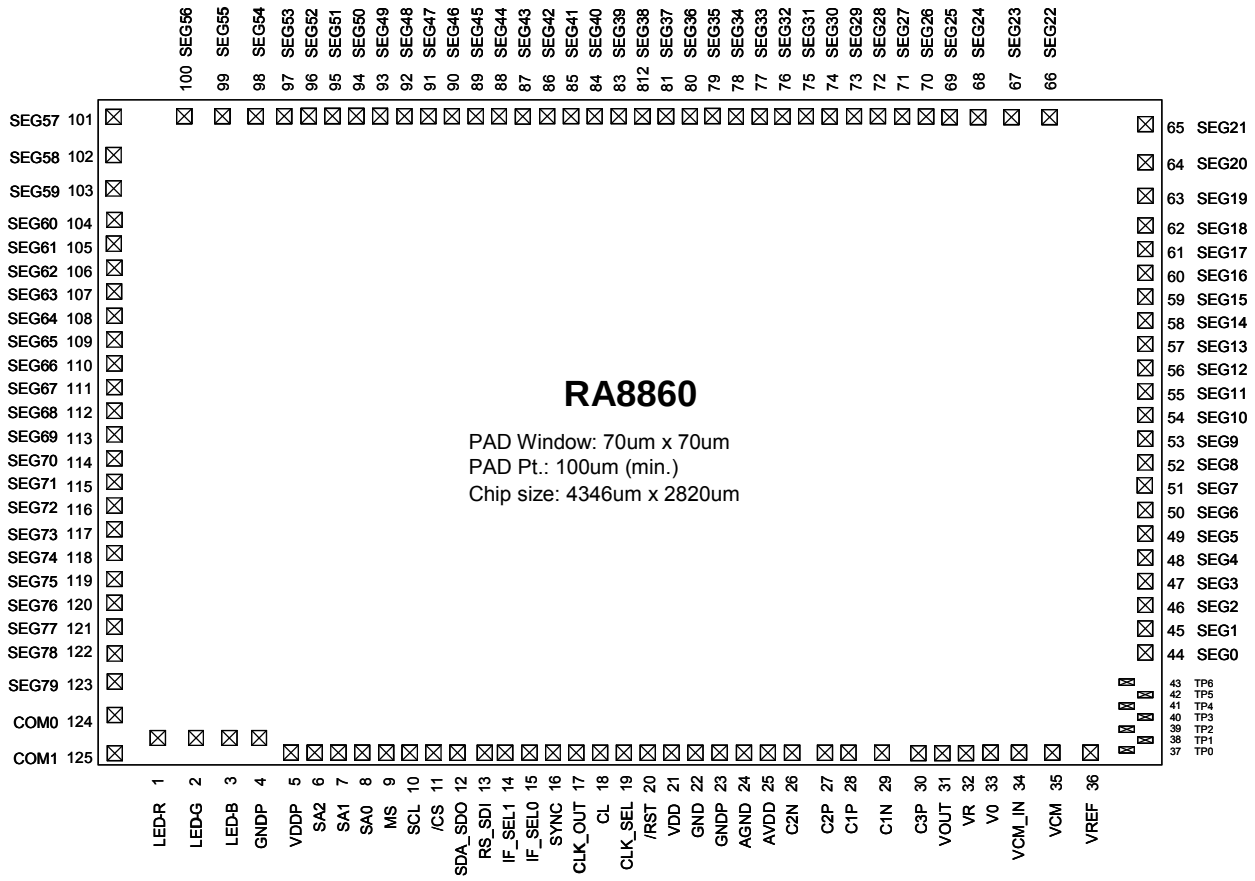


Figure 3-2 : RA8860 PAD Diagram

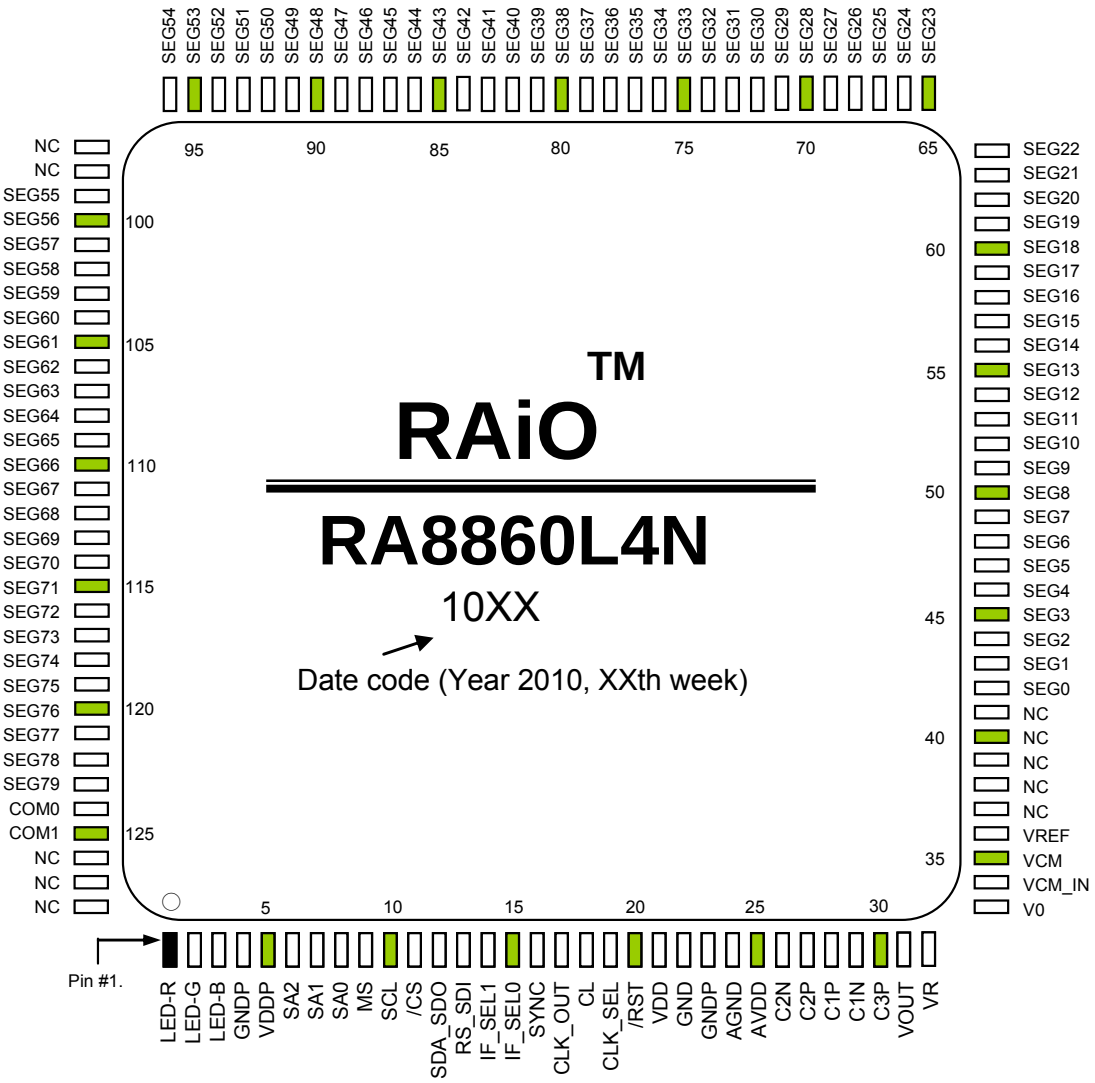


Figure 3-3 : RA8860 LQFP-128 Pin Assignment

Table 3-1 : Ordering Information

Parts Number	Package Type
RA8860	Bare Die
RA8860L4N	LQFP-128pin

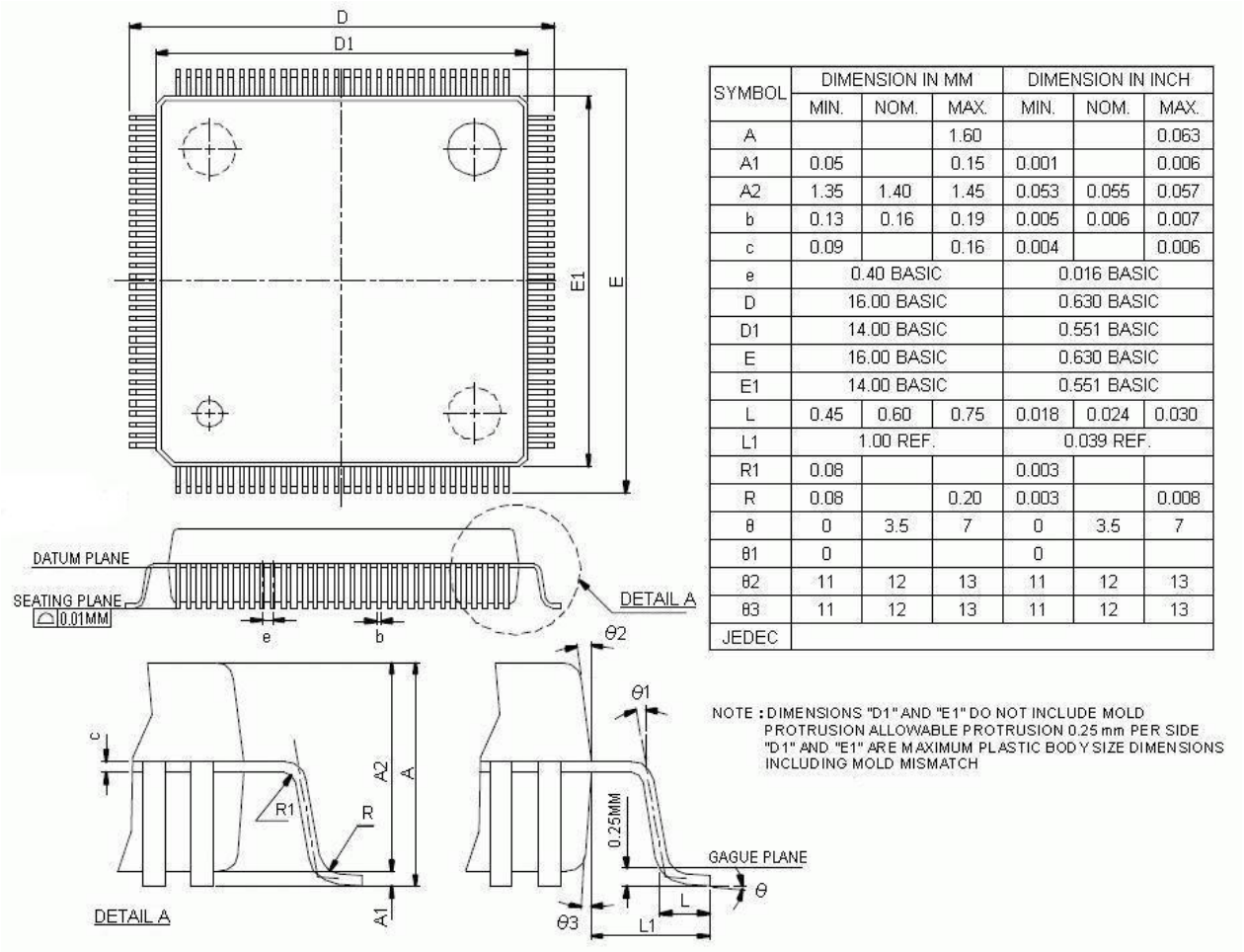
3-3 PAD Center Coordinates

Pad No.	Pad Name	X-axis	Y-axis
1	LED-R	-1836.585	-1210.29
2	LED-G	-1686.585	-1210.29
3	LED-B	-1556.145	-1210.29
4	GNDP	-1440.925	-1210.29
5	VDDP	-1250.925	-1274.97
6	SA2	-1150.925	-1274.97
7	SA1	-1050.925	-1274.97
8	SA0	-950.925	-1274.97
9	MS	-850.925	-1274.97
10	SCL	-750.925	-1274.97
11	/CS	-650.925	-1274.97
12	SDA_SDO	-550.925	-1274.97
13	RS_SDI	-450.925	-1274.97
14	IF_SEL1	-350.925	-1274.97
15	IF_SEL0	-250.925	-1274.97
16	SYNC	-150.925	-1274.97
17	CLK_OUT	-50.925	-1274.97
18	CL	49.075	-1274.97
19	CLK_SEL	149.075	-1274.97
20	/RST	249.075	-1274.97
21	VDD	349.075	-1274.97
22	GND	449.075	-1274.97
23	GNDP	549.075	-1274.97
24	AGND	649.075	-1274.97
25	AVDD	749.075	-1274.97
26	C2N	849.075	-1274.97
27	C2P	970.315	-1260.87
28	C1P	1070.315	-1260.87
29	C1N	1191.555	-1267.97
30	C3P	1312.795	-1260.87
31	VOUT	1412.795	-1260.87
32	VR	1512.795	-1260.87
33	V0	1612.795	-1260.87
34	VCM_IN	1722.795	-1260.87
35	VCM	1847.795	-1260.87
36	VREF	1997.795	-1274.97
37	TP0	2099.7	-1226.8
38	TP1	2133.0	-1184.0
39	TP2	2099.7	-1141.2
40	TP3	2133.0	-1098.4
41	TP4	2099.7	-1055.6
42	TP5	2133.0	-1012.8
43	TP6	2099.7	-970.0
44	SEG0	2113.0	-900.0

Pad No.	Pad Name	X-axis	Y-axis
45	SEG1	2113.0	-800.0
46	SEG2	2113.0	-700.0
47	SEG3	2113.0	-600.0
48	SEG4	2113.0	-500.0
49	SEG5	2113.0	-400.0
50	SEG6	2113.0	-300.0
51	SEG7	2113.0	-200.0
52	SEG8	2113.0	-100.0
53	SEG9	2113.0	0.0
54	SEG10	2113.0	100.0
55	SEG11	2113.0	200.0
56	SEG12	2113.0	300.0
57	SEG13	2113.0	400.0
58	SEG14	2113.0	500.0
59	SEG15	2113.0	600.0
60	SEG16	2113.0	700.0
61	SEG17	2113.0	800.0
62	SEG18	2113.0	900.0
63	SEG19	2113.0	1010.0
64	SEG20	2113.0	1135.0
65	SEG21	2113.0	1285.0
66	SEG22	1785.0	1350.0
67	SEG23	1635.0	1350.0
68	SEG24	1510.0	1350.0
69	SEG25	1400.0	1350.0
70	SEG26	1300.0	1350.0
71	SEG27	1200.0	1350.0
72	SEG28	1100.0	1350.0
73	SEG29	1000.0	1350.0
74	SEG30	900.0	1350.0
75	SEG31	800.0	1350.0
76	SEG32	700.0	1350.0
77	SEG33	600.0	1350.0
78	SEG34	500.0	1350.0
79	SEG35	400.0	1350.0
80	SEG36	300.0	1350.0
81	SEG37	200.0	1350.0
82	SEG38	100.0	1350.0
83	SEG39	0.0	1350.0
84	SEG40	-100.0	1350.0
85	SEG41	-200.0	1350.0
86	SEG42	-300.0	1350.0
87	SEG43	-400.0	1350.0
88	SEG44	-500.0	1350.0

Pad No.	Pad Name	X-axis	Y-axis
89	SEG45	-600.0	1350.0
90	SEG46	-700.0	1350.0
91	SEG47	-800.0	1350.0
92	SEG48	-900.0	1350.0
93	SEG49	-1000.0	1350.0
94	SEG50	-1100.0	1350.0
95	SEG51	-1200.0	1350.0
96	SEG52	-1300.0	1350.0
97	SEG53	-1400.0	1350.0
98	SEG54	-1510.0	1350.0
99	SEG55	-1635.0	1350.0
100	SEG56	-1785.0	1350.0
101	SEG57	-2113.0	1285.0
102	SEG58	-2113.0	1135.0
103	SEG59	-2113.0	1010.0
104	SEG60	-2113.0	900.0
105	SEG61	-2113.0	800.0
106	SEG62	-2113.0	700.0
107	SEG63	-2113.0	600.0

Pad No.	Pad Name	X-axis	Y-axis
108	SEG64	-2113.0	500.0
109	SEG65	-2113.0	400.0
110	SEG66	-2113.0	300.0
111	SEG67	-2113.0	200.0
112	SEG68	-2113.0	100.0
113	SEG69	-2113.0	0.0
114	SEG70	-2113.0	-100.0
115	SEG71	-2113.0	-200.0
116	SEG72	-2113.0	-300.0
117	SEG73	-2113.0	-400.0
118	SEG74	-2113.0	-500.0
119	SEG75	-2113.0	-600.0
120	SEG76	-2113.0	-700.0
121	SEG77	-2113.0	-800.0
122	SEG78	-2113.0	-900.0
123	SEG79	-2113.0	-1010.0
124	COM0	-2113.0	-1135.0
125	COM1	-2113.0	-1285.0



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.001		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09		0.16	0.004		0.006
e	0.40 BASIC			0.016 BASIC		
D	16.00 BASIC			0.630 BASIC		
D1	14.00 BASIC			0.551 BASIC		
E	16.00 BASIC			0.630 BASIC		
E1	14.00 BASIC			0.551 BASIC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
R1	0.08			0.003		
R	0.08		0.20	0.003		0.008
θ	0	3.5	7	0	3.5	7
θ1	0			0		
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
JEDEC						

NOTE : DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION ALLOWABLE PROTRUSION 0.25 mm PER SIDE "D1" AND "E1" ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH

Figure 3-4 : RA8860 Outline Dimensions

4. Pin Description

Pin Name	I/O	Description
LCD Driver Outputs		
SEG[79:0]	O	LCD Segment Driver Outputs.
COM[1:0]	O	LCD Common Driver Outputs.
LED Driver Outputs		
LED-R	O	Red LED pulse signal output.
LED-G	O	Green LED pulse signal output.
LED-B	O	Blue LED pulse signal output.
MCU Interface		
/RST	I	Reset Pin.
IF_SEL[1:0]	I	Serial MCU Interface Select. 00 : I^2C. 01 : 3-wires SPI. 10 : 4-wires SPI Type-A. 11 : 4-wires SPI Type-B.
SCL, /CS	I	Serial Data Interface. In serial mode, all of the related signals are defined as below : SCL : Serial Clock. CS : Chip Select. SDA : Bi-direction Serial Data. SDO : Serial Data Out. RS : Memory/Register Cycle Select. SDI : Serial Data In.
SDA_SDO	I/O	
RS_SDI	I	
CLK_SEL	I	Clock Select. 0 : Clock source is from internal RC oscillator. 1 : Clock source is from external pin – “CL”.
CL	I	External Clock Input. When CLK_SEL=1 or Slave mode, this pin is used as external clock input. If not used, please connect to VDDP or GND.
MS	I	Master / Slave Mode Select. 0 : Slave Mode. 1 : Master Mode.
SA[2:0]	I	Device address select of I^2C interface. If not used, please connect to VDDP or GND.
SYNC	I/O	Synchronous Pin for Multi-Chips Using. When MS=1, this pin is output. When MS=0, this pin is input.
CLK_OUT	O	System Clock Output.

Pin Name	I/O	Description
Power Supply		
VDD GND	P	Core Power.
AVDD AGND	P	Analog Power for LCD.
VDDP GNDP	P	I/O Power.
C[3:1]P C[2:1]N	O	External capacitor pins for boost circuit.
VOUT	P	Boost Power Output.
VREF	P	Reference Voltage for V0.
VR	I	For using of External R2/R1.
V0 VCM_IN VCM	P	LCD Driver Voltage.
TP[6:0]	I	Test Pins. These pins must keep NC in normal mode.

5. Electrical Characteristics

5-1 Maximum Absolute Limit

Table 5-1

Characteristic	Symbol	Value	Unit	Note
Operation voltage	VDD AVDD VDDP	-0.3 - +7.0	V	*
Driver supply voltage	V0 VOUT	-0.3 – 15.0	V	*
Operation temperature	VOPR	-35 - +90	°C	*
Storage temperature	VSTG	-55 - +125	°C	*

Note : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

5-2 DC Characteristics

Table 5-2

(VDD = +5V / +3.3V ± 10%, VSS = 0V, Ta = -30 to +80°C)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit	Note
Input high voltage	V_{IH1}	–	0.55_{VDDP}	–	V_{DDP}	V	(1)
	V_{IH2}	–	$0.8V_{DDP}$	–	V_{DDP}	V	(2)
Input low voltage	V_{IL1}	–	0	–	$0.3V_{DDP}$	V	(1)
	V_{IL2}	–	0	–	$0.2V_{DDP}$	V	(2)
Output high voltage	V_{OH}	I_{OH} / I_{OL} = 8mA	$0.8V_{DDP}$	–	–	V	(3)
Output low voltage	V_{OL1}	I_{OH} / I_{OL} = 8mA	–	–	$0.2V_{DDP}$	V	(3)
	V_{OL2}	I_{OL} = 80mA	–	–	$0.2V_{DDP}$	V	(4)
Input leakage current	I_{LKG}	V_{IN} = V_{SS} ~ V_{DDP}	-1.0	–	1.0	μA	(1) (2)
Operating current	I_{DD1}	Display On	–	–	950	μA	(5)
	I_{DD2}	Display Off	–	–	450	μA	(5)

Note :

1. This condition is for input pins /RST, SCL, /CS, RS_SDI, SDA_SDO and bi-direction pin SYNC.
2. This condition is for input pins IF_SEL[1:0], CLK_SEL, CL, MS and SA[2:0].
3. This condition is for bi-direction pins SDA_SDO, SYNC and output pin CLK_OUT.
4. This condition is for LED driving pins LED-R, LED-G, LED-B.
5. Frame Frequency = 65Hz, LED output (LED-R, LED-G, LED-B) no loading.

5-3 AC Characteristics

Table 5-3 : I²C Interface

Item	Signal	Symbol	Rating		Unit
			Min.	Max.	
SCL Clock Frequency	SCL	f_{SCL}	100	400	KHz
Bus Free Time Between STOP and START	SCL/SDA_SDO	t_{BUF}	1	--	μs
Low Period of SCL Clock	SCL	t_{LOW}	200	--	ns
High Period of SCL Clock	SCL	t_{HIGH}	200	--	ns
Data Setup Time	SCL/SDA_SDO	t_{DSIIC}	100	--	ns
Data Hold Time	SCL/SDA_SDO	t_{DHIIC}	100	--	ns

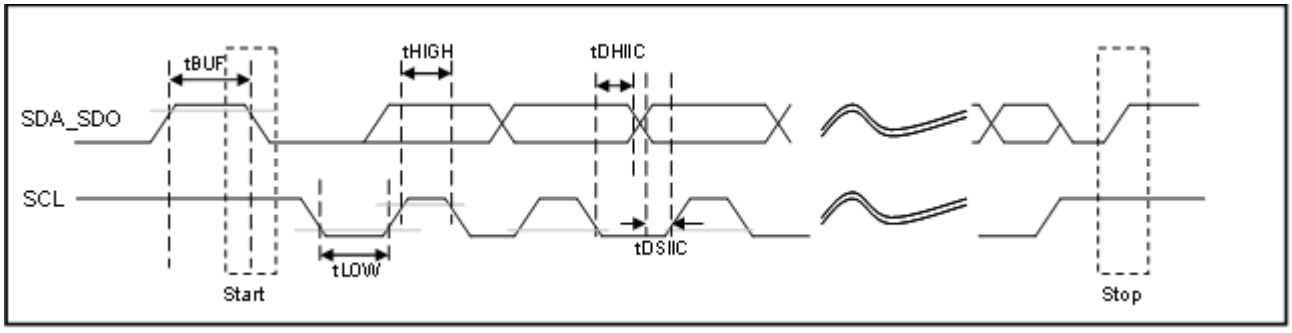


Figure 5-1 : I²C Timing

Table 5-4 : 3-Wire SPI Interface

Item	Signal	Symbol	Rating		Unit
			Min.	Max.	
Access Time	/CS	t_{CYC3}	200	--	ns
/CS Setup Time		t_{CSH3}	20	--	ns
Clock Low Pulse Width	SCL	t_{CKL3}	100	--	
Clock High Pulse Width		t_{CKH3}	100	--	
Data Setup Time	SDA_SDO	t_{DS3}	20	--	
Data Hold Time		t_{DH3}	10	--	

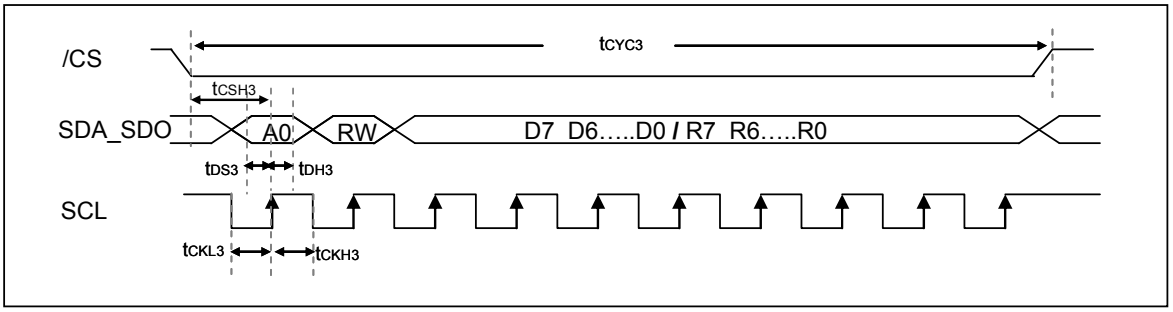


Figure 5-2 : 3-Wire SPI Timing

Table 5-5 : 4-Wire SPI (Type-A) Interface

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Access Time	$\overline{CS}$	t_{CYC4A}	--	200	--	ns
$\overline{CS}$ Setup Time		t_{CSH4}	--	20	--	ns
Clock Low Pulse Width	SCK	t_{CKL4}	--	100	--	
Clock High Pulse Width		t_{CKH4}	--	100	--	
Data Setup Time	SDA, RS	t_{DS4}	--	20	--	
Data Hold Time		t_{DH4}	--	10	--	

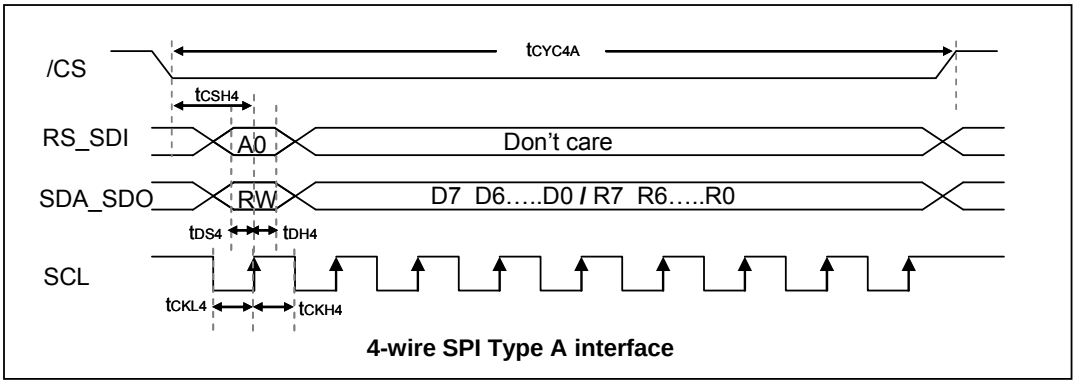


Figure 5-3 : 4-Wire SPI (Type-A) Timing

Table 5-6 : 4-Wire SPI (Type-B) Interface

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Access Time	$\overline{CS}$	t_{CYC4A}	--	200	--	ns
$\overline{CS}$ Setup Time		t_{CSH4}	--	20	--	ns
Clock Low Pulse Width	SCK	t_{CKL4}	--	100	--	
Clock High Pulse Width		t_{CKH4}	--	100	--	
Data Write Setup Time	SDI	t_{DS4}	--	20	--	
Data Write Hold Time		t_{DH4}	--	10	--	
Data Read Setup Time	SDO	t_{OS4B}	--	20	--	
Data Read Hold Time		t_{OH4B}	--	10	--	

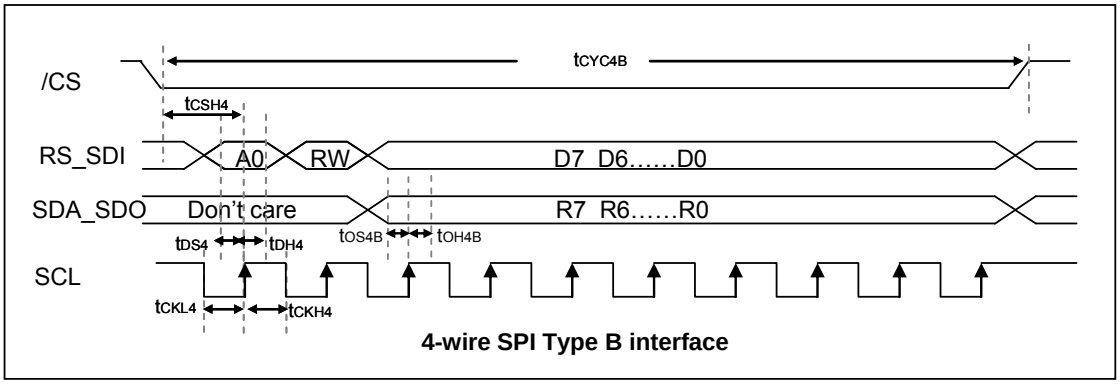


Figure 5-4 : 4-Wire SPI (Type-B) Timing

6. Register and Instruction

Table 6-1 : Registers Table

Reg No#	COMMAND	CODE									
		HEX	A0	D7	D6	D5	D4	D3	D2	D1	D0
00	NOP	00	0	0	0	0	0	0	0	0	0
01	Software Reset	01	0	0	0	0	0	0	0	0	1
10	Sleep In	10	0	0	0	0	1	0	0	0	0
11	Sleep Out	11	0	0	0	0	1	0	0	0	1
22	Exit all Point On	22	0	0	0	1	0	0	0	1	0
23	Enter all Point On	23	0	0	0	1	0	0	0	1	1
24	Blinking Setting	24	0	0	0	1	0	0	1	0	0
		-	1	0	0	0	0	0	0	0	EN
25	Blinking Address	25	0	0	0	1	0	0	1	0	1
		-	1	RBA0	CBA6	CBA5	CBA4	CBA3	CBA2	CBA1	CBA0
26	Blinking Interval	26	0	0	0	1	0	0	1	1	0
		-	1	0	0	1	0	0	BLK2	BLK1	BLK0
28	Display On	28	0	0	0	1	0	1	0	0	0
29	Display Off	29	0	0	0	1	0	1	0	0	1
2A	Set Column	2A	0	0	0	1	0	1	0	1	0
		-	1	0	0	C5	C4	C3	C2	C1	C0
2B	Set Duty	2B	0	0	0	1	0	1	0	1	1
		-	1	0	0	0	0	0	0	0	DT
2C	Memory Write	2C	0	0	0	1	0	1	1	0	0
2E	Memory Read	2E	0	0	0	1	0	1	1	1	0
2F	Address Point	2F	0	0	0	1	0	1	1	1	1
		-	1	0	RA0	CA5	CA4	CA3	CA2	CA1	CA0
A1	Red LED Start	A1	0	1	0	1	0	0	0	0	1
		-	1	LRS7	LRS6	LRS5	LRS4	LRS3	LRS2	LRS1	LRS0
A2	Green LED Start	A2	0	1	0	1	0	0	0	1	0
		-	1	LGS7	LGS6	LGS5	LGS4	LGS3	LGS2	LGS1	LGS0
A3	Blue LED Start	A3	0	1	0	1	0	0	0	1	1
		-	1	LBS7	LBS6	LBS5	LBS4	LBS3	LBS2	LBS1	LBS0
A4	Red LED Width	A4	0	1	0	1	0	0	1	0	0
		-	1	LRW7	LRW6	LRW5	LRW4	LRW3	LRW2	LRW1	LRW0
A5	Green LED Width	A5	0	1	0	1	0	0	1	0	1
		-	1	LGW7	LGW6	LGW5	LGW4	LGW3	LGW2	LGW1	LGW0
A6	Blue LED Width	A6	0	1	0	1	0	0	1	1	0
		-	1	LBW7	LBW6	LBW5	LBW4	LBW3	LBW2	LBW1	LBW0

Table 6-1 : Registers Table (Continued)

Reg No#	COMMAND	CODE									
		HEX	A0	D7	D6	D5	D4	D3	D2	D1	D0
B1	LED Mode	B1	0	1	0	1	1	0	0	0	1
		-	1	1	0	0	0	0	0	0	LEDP
B2	Frame Frequency	B2	0	1	0	1	1	0	0	1	0
		-	1	0	0	0	0	0	FR2	FR1	FR0
B7	LCD Scan Set	B7	0	1	0	1	1	0	1	1	1
		-	1	MY	0	0	0	0	0	0	0
B8	Enter Read Modify	B8	0	1	0	1	1	1	0	0	0
B9	Exit Read Modify	B9	0	1	0	1	1	1	0	0	1
BA	16 Color Set	BA	0	1	0	1	1	1	0	1	0
BB	8 Color Set	BB	0	1	0	1	1	1	0	1	1
C0	Vop Set	C0	0	1	1	0	0	0	0	0	0
		-	1	0	0	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0
D2	PWR Control	D2	0	1	1	0	1	0	0	1	0
		-	1	0	0	CK_ OEN	IRS	BST	FOL	V0	VREF
D4	RGB LED Control	D4	0	1	1	0	1	0	1	0	0
		-	1	0	0	0	0	BK	LEDR	LEDG	LEDB

[00h] NOP

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0

No operation.

[01h] Software Reset

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	1

This will cause a software reset to reset commands and registers to default, Except to REG [B2h].

[10h / 11h] Sleep Mode

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	0	0	0	SLEEP

This command causes the LCD module to enter the minimum power consumption mode. So, the functions of LCD Driver, LED Driver and RC Oscillator will be off. LCD drivers are in display off mode, output GND level. A little waiting time is needed when system is back to normal mode and users have to enable all power block circuits step by step. Please note this command will not off the LCD Power circuit like Booster and Regulator. Therefore before enter the Sleep mode, user have to off the power circuits of LCD. Refer the description of REG[D2h] and Section 7-7.

SLEEP : 0 ➔ Enter sleep mode; 1 ➔ Normal mode (Default).

[22h / 23h] All Points On/Off Mode

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	0	1	ALL

This command will display all on frame. It will not change any status and SRAM data.

ALL : 0 ➔ Exit all point on (Default); 1 ➔ Enter all point on.

[24h] Blinking Setting

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	1	0	0
1	0	0	0	0	0	0	0	EN

EN : 1 ➔ Blinking enable; 0 ➔ Blinking disable (Default).

[25h] Blinking Address

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	1	0	1
1	RBA0	CBA6	CBA5	CBA4	CBA3	CBA2	CBA1	CBA0

The register is used to set blinking address.

RBA0 : Setting the ROW blinking address. (Default = 0)

CBA[6:0] : Setting the COLUMN blinking address. (Default = 00h)

[26h] Blinking Interval

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	0	1	1	0
1	0	0	0	0	0	BLK2	BLK1	BLK0

The register is used to set blinking interval. The unit is frame and the detail setting is listed as below. (Default = 00h). The Table 6-2 also show an example of Blink Interval when Frame Rate is 75Hz.

Table 6-2

BLK[3:0]			Blink Interval (Frame)	Frame Rate = 75Hz (FR[2:0]= 001)
0	0	0	4* 1/Frame	~50ms
0	0	1	8* 1/Frame	~100ms
0	1	0	16* 1/Frame	~200ms
0	1	1	32* 1/Frame	~430ms
1	0	0	64* 1/Frame	~850ms
1	0	1	128* 1/Frame	~1.7Sec
1	1	0	256* 1/Frame	~3.4Sec
1	1	1	512* 1/Frame	~6.8Sec

[28h / 29h] Display Off Mode

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	0	0	DOFF

This command is used enter or leave display off mode. Drivers output GND level, and LED driver signals are Tri-state when system is in Display Off mode.

DOFF : 1 ➔ Display off (Default); 0 ➔ Display on.

[2Ah] Set Column

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	0	1	0
1	0	0	C5	C4	C3	C2	C1	C0

This command defines maximum column of panel. The value is from 0h to 27h (Default).

[2Bh] Set Duty

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	0	1	1
1	0	0	0	0	0	0	0	DT

This command defines the duty of panel.
DT : 0 ➔ Static; 1 ➔ 1/2 Duty. (Default)

[2Ch / 2Eh] Memory Write/Read

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	1	$\overline{W}$ /R	0

This command decides data is read from or write to memory.
$\overline{W}$ /R : 0 ➔ Write; 1 ➔ Read.

[2Fh] Address Point

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	0	1	1	1	1
1	0	RA0	CA5	CA4	CA3	CA2	CA1	CA0

This command is used to point present address. (Default = 00h)

[A1h] Red LED Start Waveform Position Setting

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	1
1	LRS7	LRS6	LRS5	LRS4	LRS3	LRS2	LRS1	LRS0

Red LED starts waveform position setting. (Default = 00h)

[A2h] Green LED Start Waveform Position Setting

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	1	0
1	LGS7	LGS6	LGS5	LGS4	LGS3	LGS2	LGS1	LGS0

Green LED starts waveform position setting. (Default = 00h)

[A3h] Blue LED Start Waveform Position Setting

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	1	1
1	LBS7	LBS6	LBS5	LBS4	LBS3	LBS2	LBS1	LBS0

Blue LED starts waveform position setting. (Default = 00h)

[A4h] Red LED Width Waveform Setting

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	1	0	0
1	LRW7	LRW6	LRW5	LRW4	LRW3	LRW2	LRW1	LRW0

Red LED width waveform setting. (Default = FFh)

[A5h] Green LED Width Waveform Setting

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	1	0	1
1	LGW7	LGW6	LGW5	LGW4	LGW3	LGW2	LGW1	LGW0

Green LED width waveform setting. (Default = FFh)

[A6h] Blue LED Width Waveform Setting

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	1	1	0
1	LBW7	LBW6	LBW5	LBW4	LBW3	LBW2	LBW1	LBW0

Blue LED width waveform setting. (Default = FFh)

[B1h] LED Mode

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	0	1
1	0	0	0	0	0	0	0	LEDP

This command is used to set LED driving mode.

LEDP : 0 ➔ The LED-R, LED-G and LED-B signals will be low active (Default);
1 ➔ The LED-R, LED-G and LED-B signals will be high active.

[B2h] Frame Frequency

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	1	0
1	0	0	0	0	0	FR2	FR1	FR0

This command is used to set frame frequency. (Default = 00h)

Table 6-3

FR[2:0]			Frame Rate (VDD=5V)
0	0	0	65Hz (default)
0	0	1	75Hz
0	1	0	85Hz
0	1	1	95Hz
1	0	0	105Hz
1	0	1	115Hz
1	1	0	125Hz
1	1	1	135Hz

[B7h] LCD Scan Set

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	1	1
1	MY	0	0	0	0	0	0	0

This command is used to set LCD scan direction.

MY : 0 ➔ COM0 to COM1 (default); 1 ➔ COM1 to COM0

[B8h / B9h] Read Modify Write Select

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	RMW

This command decide the read modify write. Normally, the counter of address will increase (+1) after execute memory read (0x2E) sequence. But when enter read modify mode, the counter will stop counting.

RMW : 0 ➔ Enter read modify write. 1 ➔ Exit read modify write (Default)

[BAh / BBh] Color Set

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	COLOR

This command decides 16 or 8 color set.

COLOR : 0 ➔ 16 color set (Does not support if panel is normally black); 1 ➔ 8 color set (default).

[C0h] Vop Set

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	0	0	0	0	0
1	0	0	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0

This command is used to set the optimum LCD voltage V0. (Default = 20h)

[D2h] PWR Control

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	1	0	0	1	0
1	0	0	CK_OEN	IRS	BST	FOL	V0	VREF

This command is used to set internal circuits enable or disable. (Default = 10h)

CK_OEN : 0 ➔ “CLK_OUT” and “SYNC” turn off, output high, 1➔ “CLK_OUT” and “SYNC” turn on.

IRS : 0 ➔ Select External R-string for Regulator, 1➔ Select Internal R-string,

BST : 0 ➔ Disable 4x boost, 1➔ Enable 4x boost.

FOL : 0 ➔ Disable LCD Bias, 1 ➔ Enable LCD Bias.

V0 : 0 ➔ Disable Regulator, 1 ➔ Enable Regulator.

VREF : 0 ➔ Select External Reference Voltage, 1 ➔ Select Internal Reference Voltage.

[D4h] RGB LED Control

A0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	1	0	1	0	0
1	0	0	0	0	BK	LEDR	LEDG	LEDB

This command is used to control RGB LED turn on or off individually.

BK : 0 ➔ All RGB LED turn off (default); 1 ➔ RGB LED turn on or off by LEDR, LEDG and LEDB bit.

Table 6-4

BK	LEDR	LEDG	LEDB	Description	
0	X	X	X	RGB LED Control off	
1	0	0	0	Backlight off	
1	0	0	1	Blue	
1	0	1	0	Green	
1	0	1	1	Cyan	
1	1	0	0	Red	
1	1	0	1	Pink	
1	1	1	0	Yellow	
1	1	1	1	White	

7. Function Description

7-1 MCU Interface

The RA8860 supports four type serial interfaces. One is 3-Wires SPI, one is I^2C mode, and the others are 4-wires SPI (Type-A, Type-B). This feature is control by the pin IF_SEL[1:0]. Refer to Table 7-1. The Table 7-2 is the pin definition of those serial modes.

Table 7-1 : MCU Interface Selection

IF_SEL[1:0]	MCU Interface
00	I^2C
01	3-Wires SPI
10	4-wires SPI, Type-A
11	4-wires SPI, Type-B

Table 7-2 : The Pin Definition of Serial Signals

Mode / Signals	I^2C	3-Wires SPI	4-wires SPI, Type-A	4-wires SPI, Type-B
SCL	Serial Clock	Serial Clock	Serial Clock	Serial Clock
/CS	Note*	Chip Select	Chip Select	Chip Select
SDA_SDO	Bi-direction Data	Bi-direction Data	Bi-direction Data	Data Out
RS_SDI	Note*	Note*	A0	Data In
SA[2:0]	Device Address	Note*	Note*	Note*

Note : Please connect to VDDP or GND.

7-1-1 I²C Interface

If use I²C mode, the MCU only need two signals to connect with RA8860 – "SCL" and "SDA_SDO". The "SDA_SDO" include Device Address, A0, Read/Write State(RW), ACK and Data that synchronize with clock signal – "SCL". The hardware input "SA[2:0]" are device addressing pins and should be tied to high or low. Once the hardware setting of "SA[2:0] are same with the device address of "SDA_SDO", then the RA8860 is active. So there are 8 devices that could be decoded by SA[2:0].

For exampls, the Figure 7-2 SA2 connect to VDDP; SA1 and SA0 connect to GND. So the device address of SA[2:0] is 2'100b. Therefore the completed device address of I²C bus is :

AD = { 2'b10, SA[2:0], 1'b0}

= 6'b101000

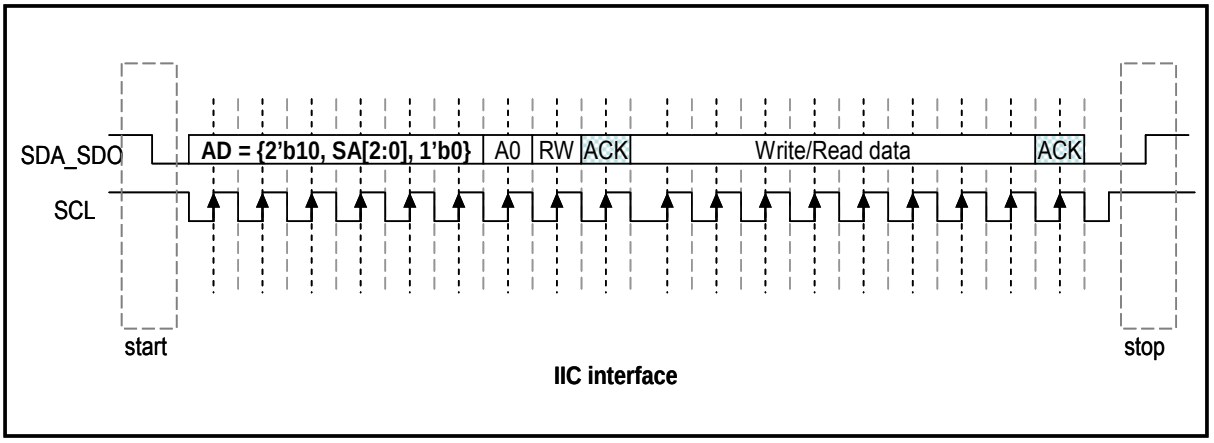


Figure 7-1 : I²C Interface Timing

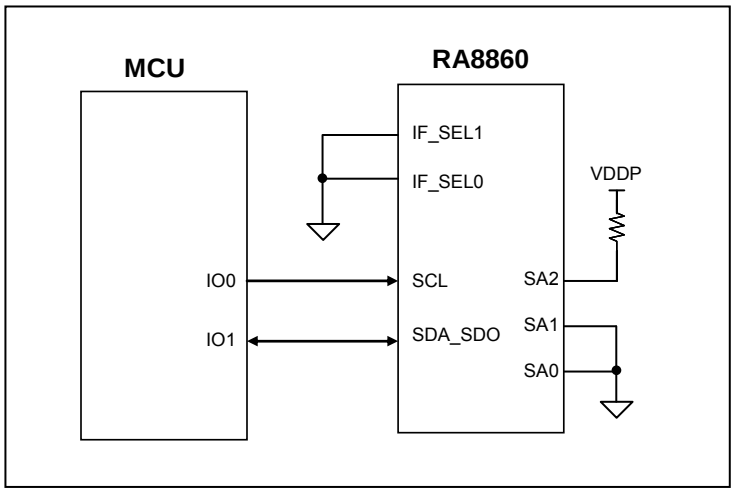


Figure 7-2 : I²C Interface to MCU

7-1-2 3-Wires SPI

In 3-Wires SPI mode, the “SDA_SDO” include A0, Read/Write State(RW) and Data that synchronize with clock signal – “SCL”. The “SDA_SDO” is a bi-direction pin. Normally it output, but when RW=1, this pin is become input in data state.

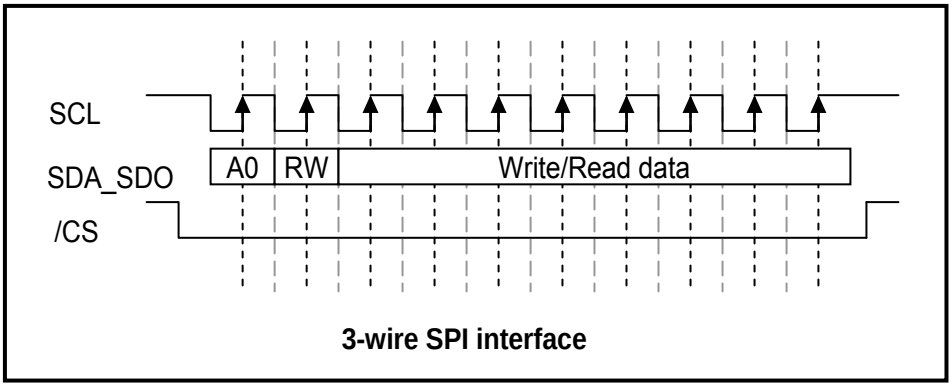


Figure 7-3 : 3-Wires SPI Timing

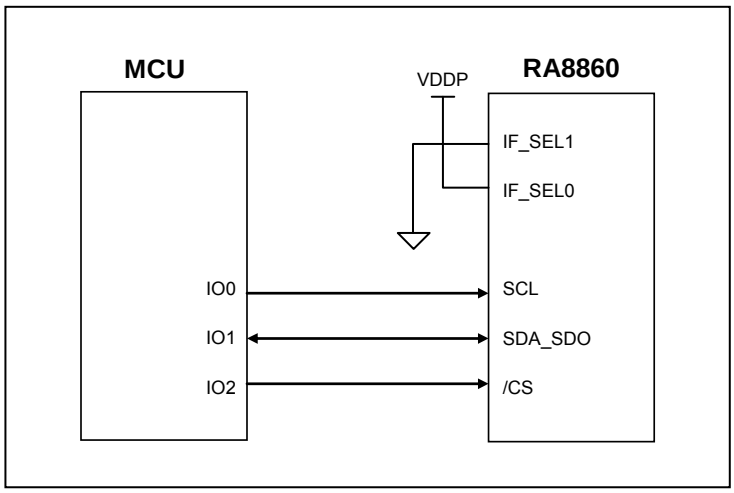


Figure 7-4 : 3-Wires SPI Interface to MCU

7-1-3 4-wires SPI / Type-A

The 4-wires(Type-A) SPI is very similar to 3-Wires SPI mode. The difference is only A0 state move to pin “RS_SDI”. The “SDA_SDO” is a bi-direction pin. Normally it output, but when RW=1, this pin is become input in read data state.

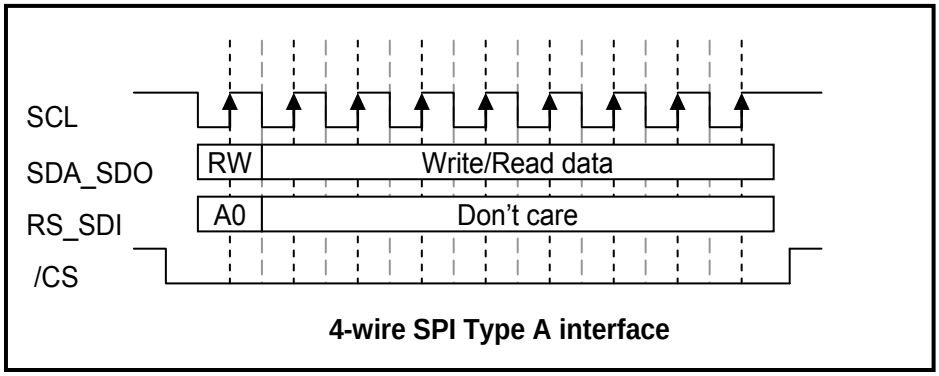


Figure 7-5 : 4-wires SPI (Type-A) Timing

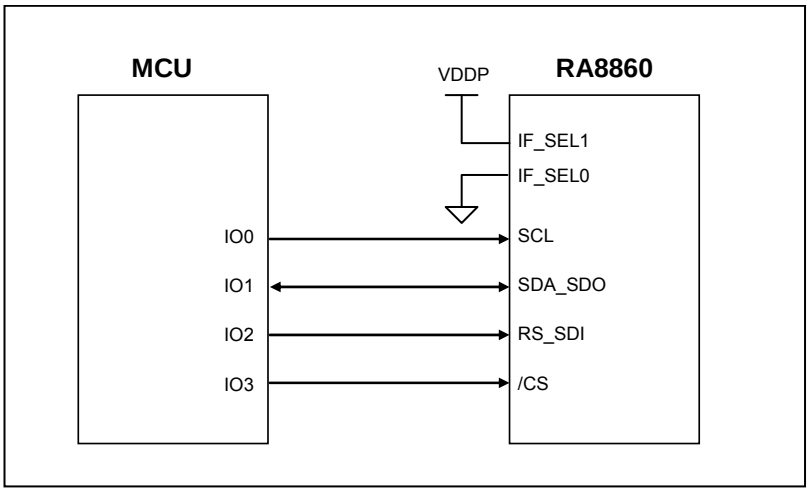


Figure 7-6 : 4-wires SPI Type-A Interface to MCU

7-1-4 4-wires SPI / Type-B

The 4-wires(Type-B) SPI is also similar to 3-Wires SPI mode. The “RS_SDI” is input pin include A0, Read Write State (RW) and write Data that synchronize with clock signal – “SCL”. The “SDA_SDO” is data output pin. When RW=1, the MCU could read serial data of RA8860 from “SDA_SDO”

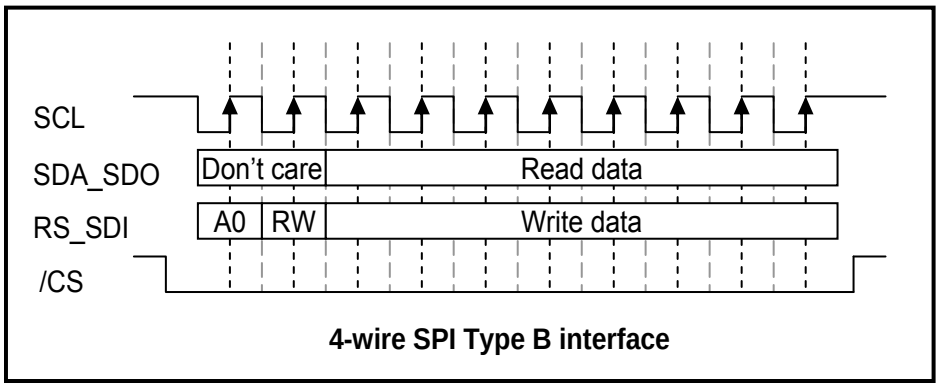


Figure 7-7 : 4-wires SPI (Type-B) Timing

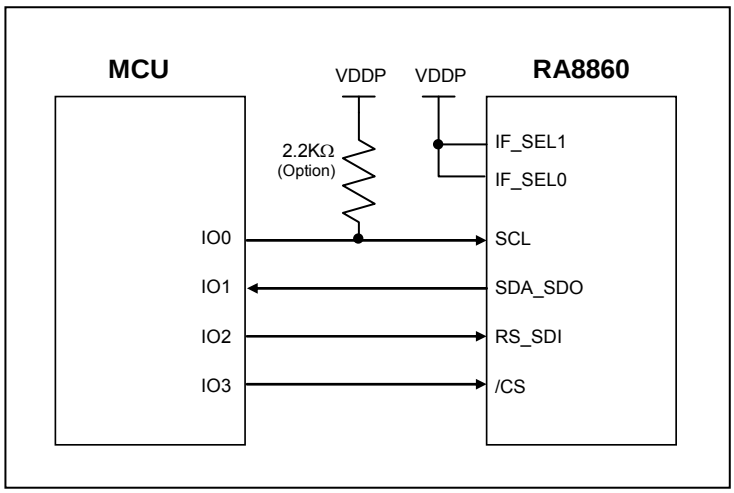
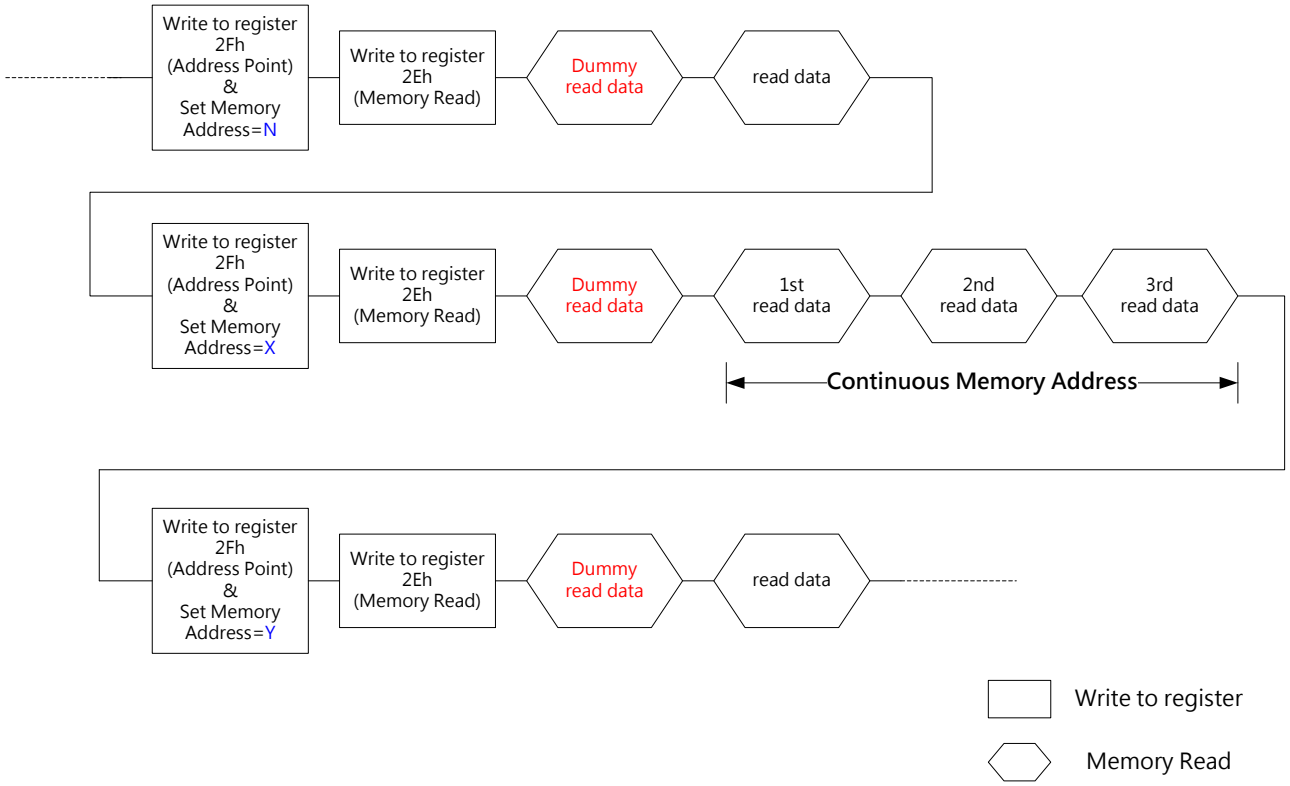


Figure 7-8 : 4-wires SPI Type-B Interface to MCU

7-1-5 Memory Read



Example:

```
LCD_CmdWrite(0x2F);      //Set Memory Address=N
LCD_DataWrite(N);

LCD_CmdWrite(0x2E);      //Memory Read

Temp=LCD_DataRead();     //Dummy Read
Temp=LCD_DataRead();     //Data


LCD_CmdWrite(0x2F);      //Set Memory Address=X
LCD_DataWrite(X);

LCD_CmdWrite(0x2E);      //Memory Read

Temp=LCD_DataRead();     //Dummy Read
Temp=LCD_DataRead();     //1st Data
Temp=LCD_DataRead();     //2nd Data
Temp=LCD_DataRead();     //3rd Data

LCD_CmdWrite(0x2F);      //Set Memory Address=Y
LCD_DataWrite(Y);

LCD_CmdWrite(0x2E);      //Memory Read

Temp=LCD_DataRead();     //Dummy Read
Temp=LCD_DataRead();     //Data
```

Figure 7-9 : Memory Read

7-2 Master Slave Mode

RA8860 supports multi-chip using as serial connected and is realized by setting hardware pins “MS”. When “MS” connects to High, the RA8860 works as a Master, and outputs synchronous signals from “SYNC” and “CLK_OUT” to Slave. When “MS” connects to Low, the RA8860 works as a Slave, and “CL” is clock input which receives clock from Master’s “CLK_OUT”. And “SYNC” is input that receives synchronous signals from Master’s “SYNC”. The maximum cascade level is eight, that means the maximum resolution of LCD panel could be supported is 80x2x8. The cascade function supports four type serial interfaces.

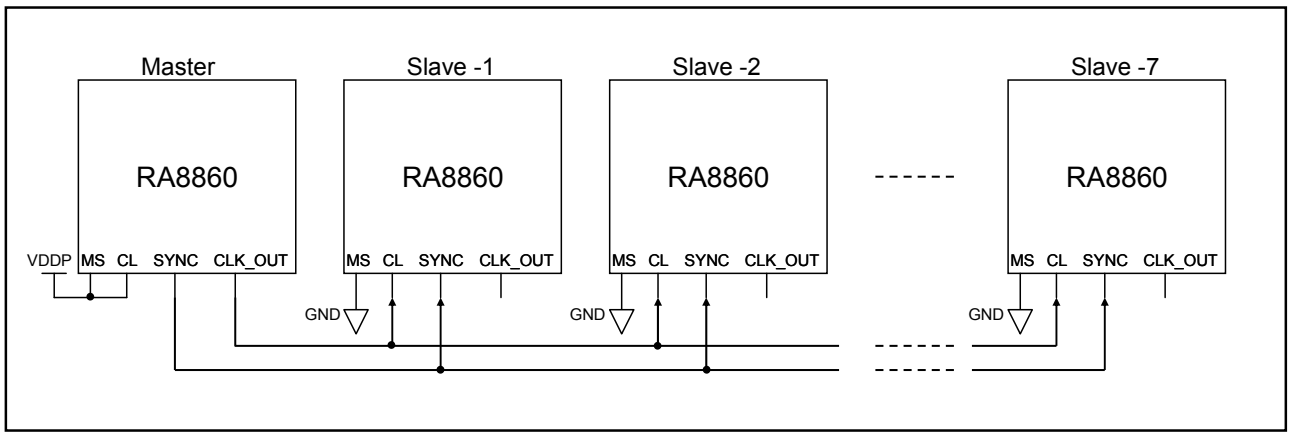


Figure 7-10 : Master and Slave Mode

Figure 7-11 is an example for 3-wire SPI to master and slave connection. The “CLK”,“SDA_SDO”, and “/RST” all of the RA8860 are connected together which from one driving source of MCU. The “/CS” is driven by MCU individually. If user wants to use I^2C interface for master and slave mode, please refer to Figure 8-3 for detail.

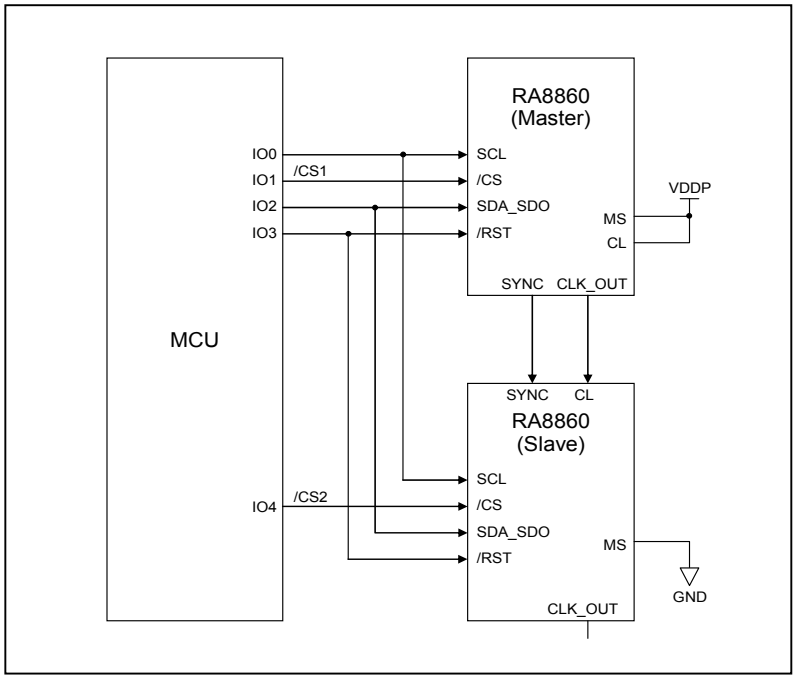


Figure 7-11 : MCU 3-wire SPI Interface to Master and Slave

7-3 Clock and Internal RC-Oscillator

The system clock of RA8860 is from internal RC-Oscillator or external clock source. When pin "CLK_SEL" is Low, the clock source is from internal RC-Oscillator. When "CLK_SEL" is High, the clock source is from pin "CL", and internal RC-Oscillator will be off.

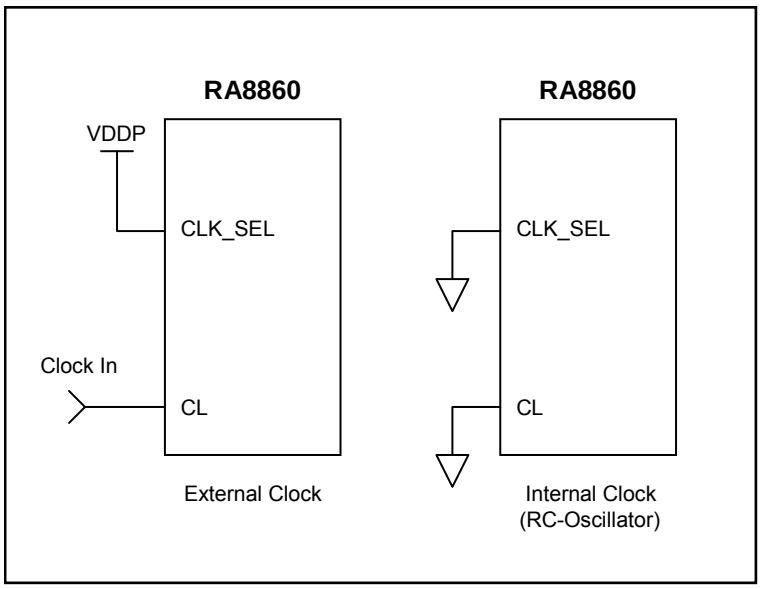


Figure 7-12 : Internal / External Clock

As above description, when pin "CLK_SEL" is Low, the internal RC-Oscillator is enabled and generates the system clock of RA8860. The system clock frequency is adjustable by bit FR[2:0] setting of REG [B2h]. RA8860 provides 8 stages tuning to control RC-Oscillator frequency. The relation between System Clock and Frame Rate is listed in the following table.

Table 7-3

FR[2:0]			Frame Rate	System Clock
0	0	0	65Hz	200KHz
0	0	1	75Hz	230KHz
0	1	0	85Hz	260KHz
0	1	1	95Hz	290KHz
1	0	0	105Hz	325KHz
1	0	1	115Hz	350KHz
1	1	0	125Hz	380KHz
1	1	1	135Hz	415KHz

7-4 Display Data

Each segment output is composed by 4bit data to implement 16 colors. So, the internal 8-bit data from MCU bus can deliver 2 segment data. The 4-bit data can represent 16 colors as the color set table. The 16 colors or 8 colors mode could be set by LSB of REG [BAh]. When 8 colors mode is set, the MSB of each nibble will be ignored. All 80x2x4 bits data are read from display RAM or register once and CORE circuit will transfer the data to COMn and SEGn signals.

7-4-1 Display Data RAM

It is 80x2x4 bits capacity RAM prepared for storing dot data. Refer to the following memory map for the RAM Configuration.

Table 7-4 : Display Data RAM

			RAM Alignment																						
			Column																						
			39								38								-----		0				
			←																						
Row	MY=0	MY=1	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0	------	D7	D6	D5	D4	D3	D2	D1	D0	COM out
	0	1	Display data				Display data				Display data				Display data				------	Display data				Display data				COM0
	1	0	Display data				Display data				Display data				Display data				------	Display data				Display data				COM1
SEG out			SEG79				SEG78				SEG77				SEG76				------	SEG1				SEG0				

7-4-2 8 Color Data Format

SEG	SEGn+1				SEGn			
Data	X	D6	D5	D4	X	D2	D1	D0

Table 7-5 : 8-Colors Table (Normally White)

Data	Color	
000	White	
001	Yellow	
010	Pink	
011	Red	
100	Cyan	
101	Green	
110	Blue	
111	Black	

Table 7-6 : 8-Colors Table (Normally Black)

Data	Color	
111	White	
110	Yellow	
101	Pink	
100	Red	
011	Cyan	
010	Green	
001	Blue	
000	Black	

7-4-3 16 Color Data Format

SEG	SEGn+1				SEGn			
Data	D7	D6	D5	D4	D3	D2	D1	D0

Table 7-7 : 16-Colors Table (Normally White)

Data	Color		Data	Color	
0000	White		1000	Maroon	
0001	Yellow		1001	Aqua	
0010	Pink		1010	Lime Green	
0011	Red		1011	Teal	
0100	Purplish Red		1100	Green	
0101	Light Green		1101	Blue	
0110	Orange		1110	Navy Blue	
0111	Purple		1111	Black	

7-5 Blinking Function

RA8860 supports the blinking function for each dot. User just needs to set the blinking frequency (REG [26h]) and which dot (REG [25h]) that will blink, and then enables (REG [24h]) it. This dot will blink according to the setting data. If user wants to stop blinking of the point, just sets the point address and disables it.

7-6 Reset

The RA8860 requires a reset pulse at least 1ms after power-on in order to re-initialize its internal state. The Figure 7-13 (1) is an example circuit of "/RST" pin. When pin "/RST" connects to Low, or execute Software Reset Instruction, it will initialize internal circuit and the following procedures are occurred.

- Display off ➔ SEG / COM output VSS (GND) level
- Display all points off
- The LCD power supply circuit is stopped
- RC-Oscillator is stopped

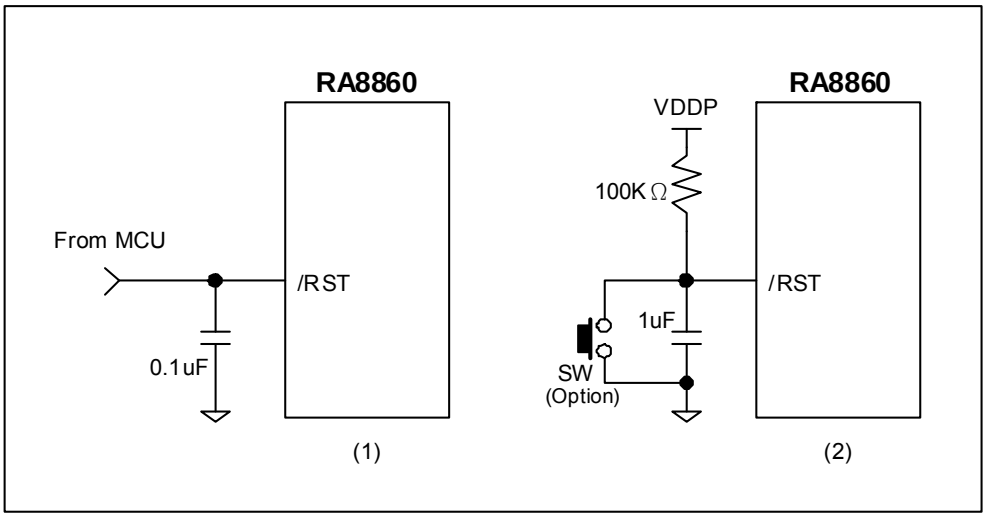


Figure 7-13 : Example Circuit of /RST Pin

7-7 LCD Bias and Power

The LCD Driver power system operation method is described as bellow in Figure 7-14. The power supply system is a low power consumption circuit for LCD. It is consisted of Booster, Reference voltage, Voltage Regulator and Voltage Follower circuits.

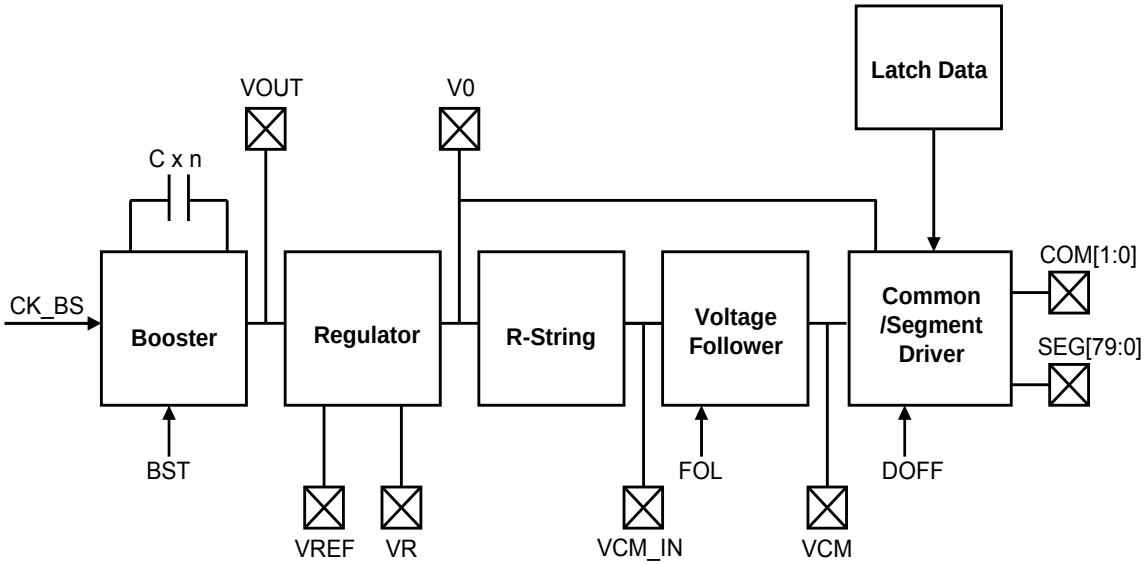


Figure 7-14 : LCD Driver and Power Supply Circuit Block

User can select either the internal or external power by setting REG [D2h]. Please refer the following Table 7-8 to control power system.

Table 7-8 : Setting Table of Power Circuit

Driver Control Register [D2h] D3 D2 D1 D0	Booster (BST)	Voltage Follower (FOL)	Voltage Regulator (V0)	Reference Voltage (VREF)	External Power
1 1 1 1	ON	ON	ON	Internal	VDD
0 1 1 1	OFF	ON	ON	Internal	VOUT, VDD
1 1 1 0	ON	ON	ON	External	VREF, VDD
0 1 1 0	OFF	ON	ON	External	VOUT, VREF, VDD
0 1 0 0	OFF	ON	OFF	Don't Need	V0, VDD
0 0 0 0	OFF	OFF	OFF	Don't Need	V0, VCM, VDD

7-7-1 Booster Circuit

The Booster circuit is embedded in RA8860 to provide higher voltage than VDD for LCD using. It can generate 2x, 3x or 4x step-up of "VDD - GND" voltage levels. When "VOUT" pin is equal to 2×VDD, the capacitor C1 is connected between C1P and C1N; when "VOUT" is equal to 3×VDD, an additional capacitor C1 is connected between C2P and C2N; and when "VOUT" is equal to 4×VDD, one more additional capacitor is connected between C3P and C1N.

When the circuit operates in 2x or 3x mode, the unused positive capacitor pins (CxP) must be connected to VOUT in short circuit and negative pins (CxN) are kept floating. The detail application circuit is shown as below Figure 7-15.

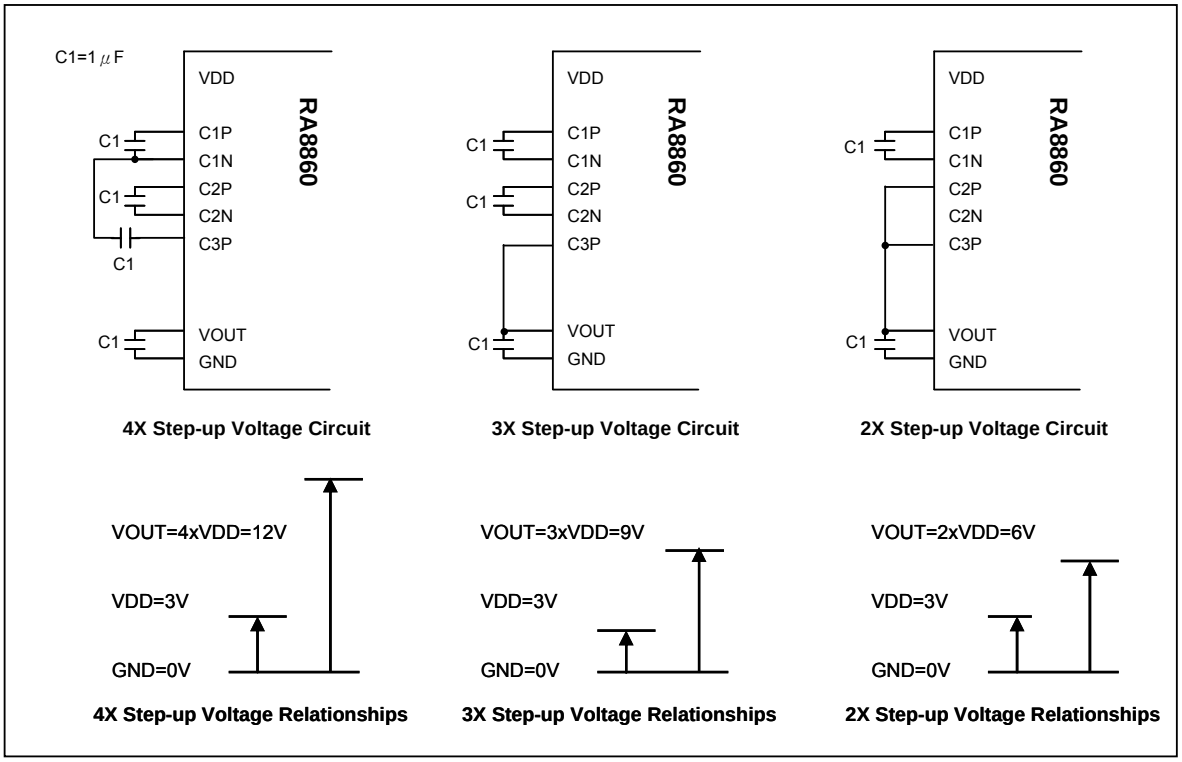


Figure 7-15 : Application Circuit of Booster

The clock source of Booster is from system clock and also controlled by REG [B2h]. The clock will be divided by four internally to be real clock used by Booster.

Normally, if only internal power is used, please refer the application circuit in Figure 7-16. If external VOUT is used, that means do not use the internal Booster, then the connection is shown as Figure 7-17.

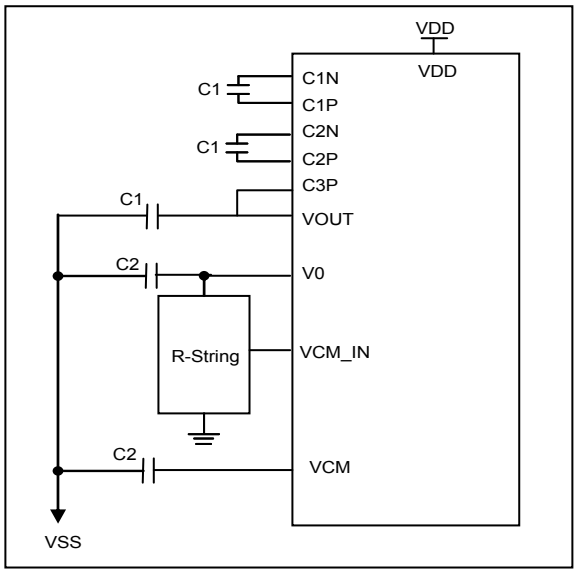


Figure 7-16 : Internal VOUT (3xVDD)

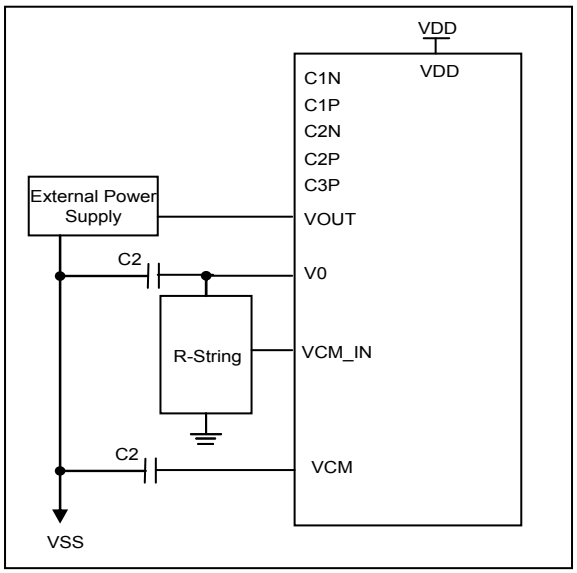


Figure 7-17 : External VOUT

7-7-2 Voltage Regulator

The Voltage Regulator is consisted of Bandgap reference voltage circuit and non-inverting OP-Amp.The Bandgap circuit generates a nearly 2.1V reference voltage and provide for the non-inverting OP-Amp (Figure 7-18). If the bit4 (IRS) of REG [D2h] is 1, then the formula of V_0 is derived as following :

$$V0 = (2+\alpha/21) * V_{REF}$$

V_{REF} is the output voltage of Bandgap reference circuit. The coefficient α is the setting of Vop[5:0] of REG [C0h] that controls a built-in 64-level adjustment circuit. V0 could be adjusted from 4.2V to 10.5V and each step is about 0.1V. The default output voltage is 7.4V (α =32).

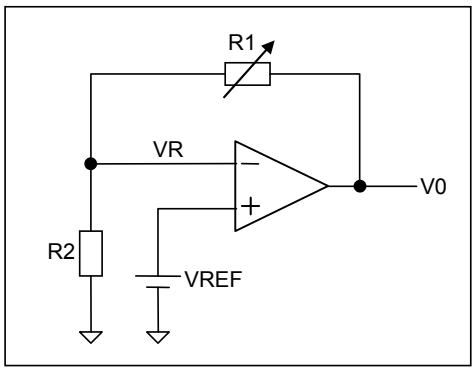


Figure 7-18 : Voltage Regulator

Table 7-9 : Select V_{REF}

V_{REF} Type	REG [D2h] D1 (V0)	REG [D2h] D0 (VREF)	V_{REF}
Internal V_{REF}	1	1	Internal V_{REF}
External V_{REF}	1	0	V_{REF} Pin

The V_{REF} of RA8860 is supplied from internal circuit or external V_{REF} Pin. Please refer Table 7-9. If user wants to get specific resistor ratio by using external resistor divider, the internal R-string could be disabled by setting bit 4 of REG [D2h] and the external circuit is show in Figure 7-19.

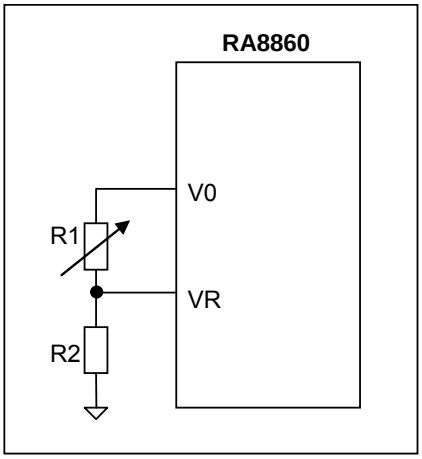


Figure 7-19 : Use External Resistor Divider

If the bit4 (IRS) of REG [D2h] is 0, then the formula of V0 is derived as following :

$$V0 = (R1+R2) / R2 * V_{REF}$$

7-7-3 Voltage Follower

The embedded voltage follower provides VCM level for COM driver using.The bias voltage is divided by external R-string and input from VCM_IN pin to provides VCM power. Of course, user can select internal or external LCD bias circuit to supply VCM and the circuit is shown as Figure 7-20 and Figure 7-21. Please refer Table 7-8 to control the power status. In any case, the relationship of VOUT, V0, VCM, and GND is shown as following :

VOUT > V0 > VCM > GND

Figure 7-20 shows the circuit that uses internal voltage follower. For use external V0 and VCM, the connection is shown as Figure 7-21.

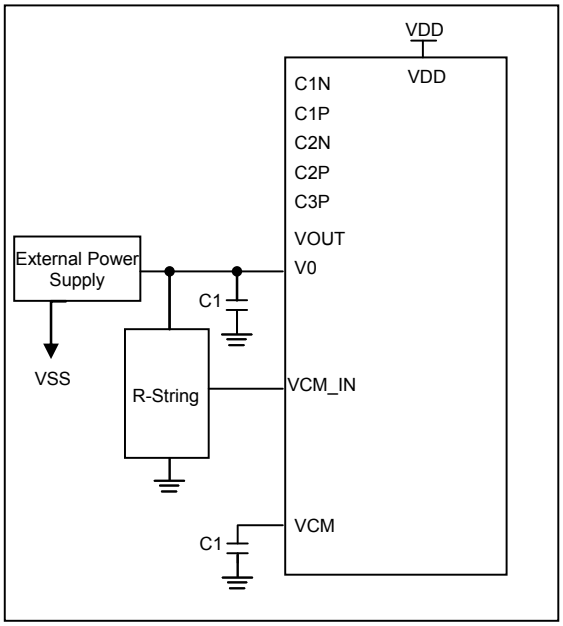


Figure 7-20 : Use Internal Voltage Follower

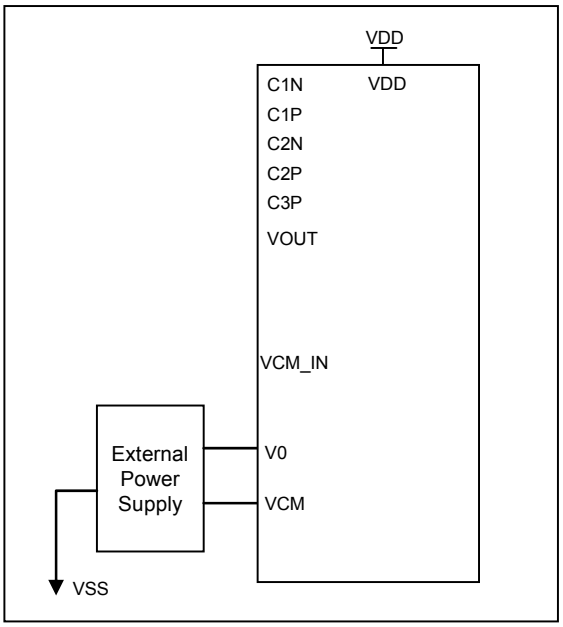


Figure 7-21 : Use External Voltage Follower

7-8 LCD Driver

The Segment/Common Driver of RA8860 is used to latch the data of pre-stage, then send to Level Shifter for combination. The combined data will follow the Timing Generator to control the switchs then pass the V0, VCM and GND to Common and Segment. All driver cells output GND when display off is active. The RA8860 provids 80 Segments and 2 Commons driver output that means total 160 pixel resolution.

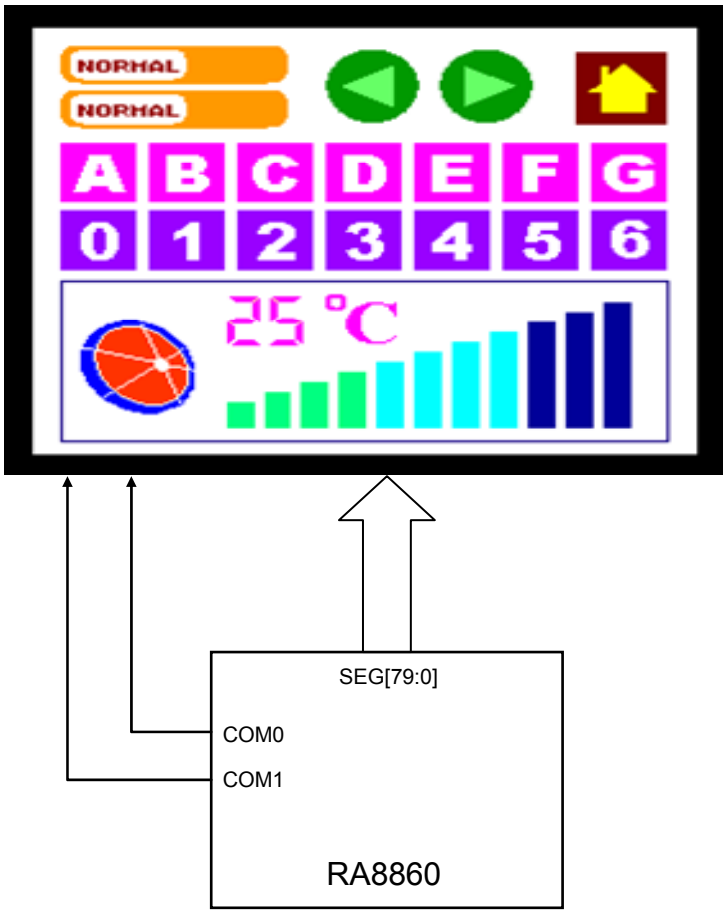


Figure 7-22 : LCD Driving Interface

7-9 LED Driver

RA8860 supports three LED driving signals to LED backlight. The “LED-R”, “LED-G” and “LED-B” pins are high driving output. User could drive the LED directly or through Tansistor(BJT). The following Figure 7-23 and Figure 7-24 are two examples of application circuit. The active level of pins “LED-R”, “LED-G” and “LED-B” is controled by REG [B1h].

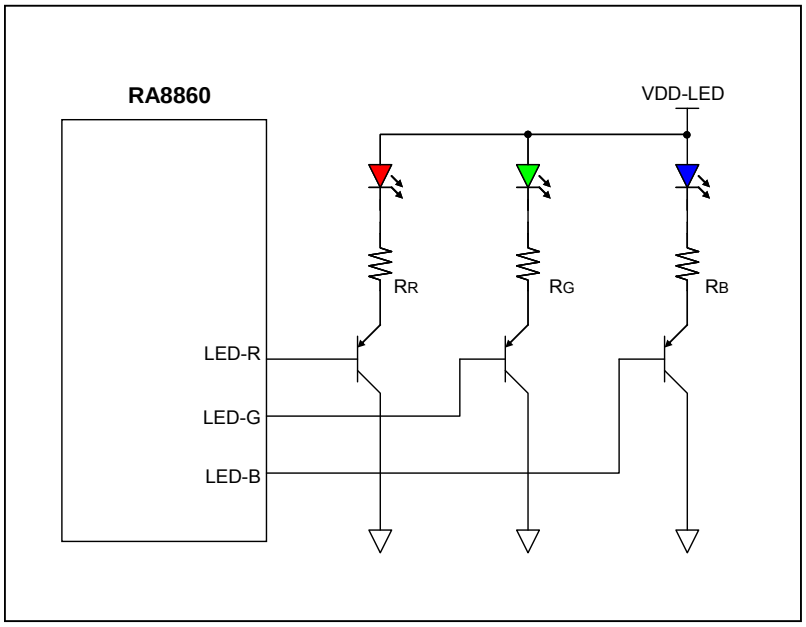


Figure 7-23 : LED Driving Circuit -1

In Figure 7-24, the maximum sink current of each LED driving pin is 80mA. Please note that base on FSLCD principle, the RGB LEDs are sequence turn on. And only one LED channel is turn on in same period. So user have to use limited current resistor R to keep current less than 80mA at each pin to avoid unexpected problems. And do not turn on the RGB LED at same period.

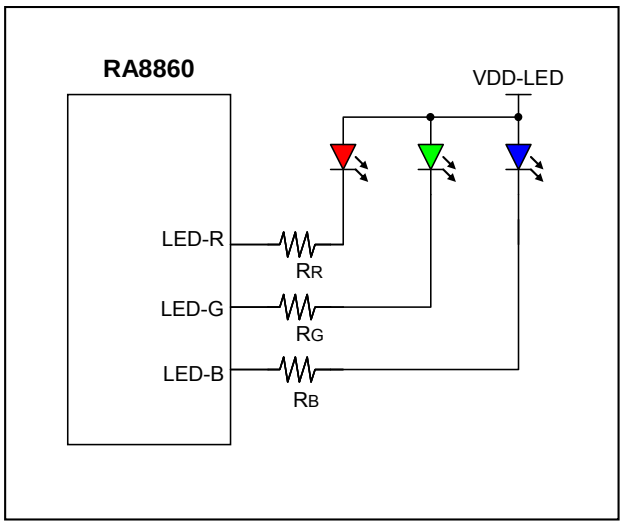


Figure 7-24 : LED Driving Circuit -2

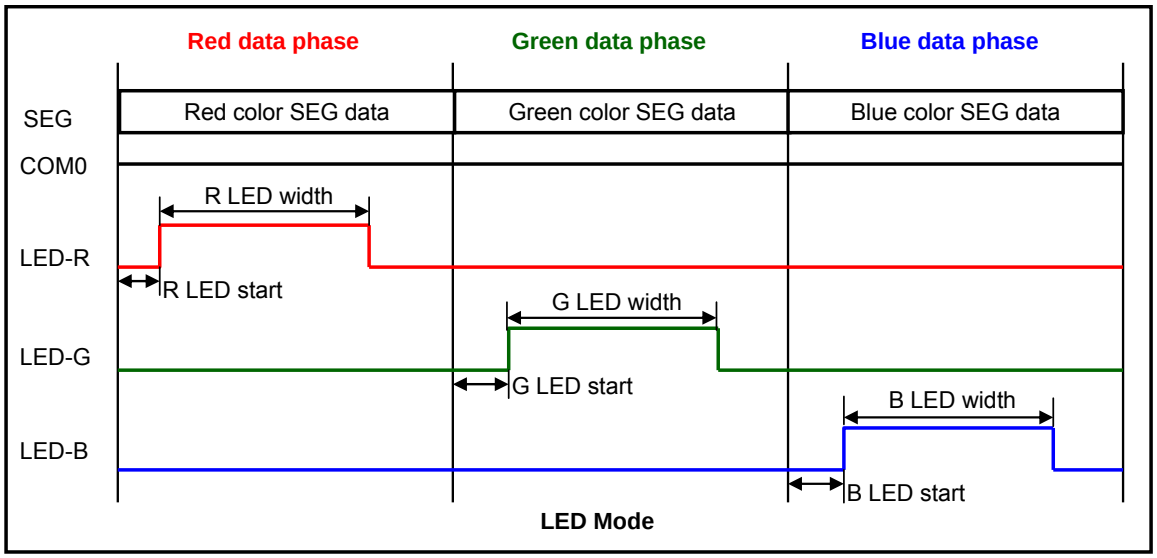


Figure 7-25 : LED Timing Control

The LED tune on or turn off is controlled by REG [D4h]. In each LED phase, the turn on time and active time (width) are controlled by individual register. Please refer above Figure 7-25. The start turn position is set by REG [A1h~A3h]. Active time is set by REG [A4h~A6h].

7-10 Output Status of Reset & Sleep

Table 7-10 : Signal State of Reset and Sleep

Signal	Reset	Sleep
SDA_SDO	when IF_SEL[1:0] = 11, output high.	when IF_SEL[1:0] = 11, keep output.
COM[1:0]	output low	output low
SEG[79:0]	output low	output low
LED-R LED-G LED-B	Tri-state	Tri-state
SYNC	when MS=1, output high. (Note*)	when MS=1 & CK_OEN=0, output high. when MS=1 & CK_OEN=1, output. (Note*)
CLK_OUT	output high	output high

Note : When MS=0, this pin is input.

8. Application Circuit

The following figures are application circuits of RA8860. Figure 8-1 uses 3.3V power and 2X Booster for VOUT, and uses I²C mode MCU interface. The LCD voltage (V0) is set by REG [C0h], and users have to select internal R-string and reference voltage by REG [D2h] because there is no reference voltage and resistor is needed in this case.

If the LCD voltage is 5V then Figure 8-2 is an example of using 5V power application. In this case the MCU interface is 3-wire SPI, so signal "IF_SEL1" is connected to GND, and IF_SEL0 is connected to VDD.

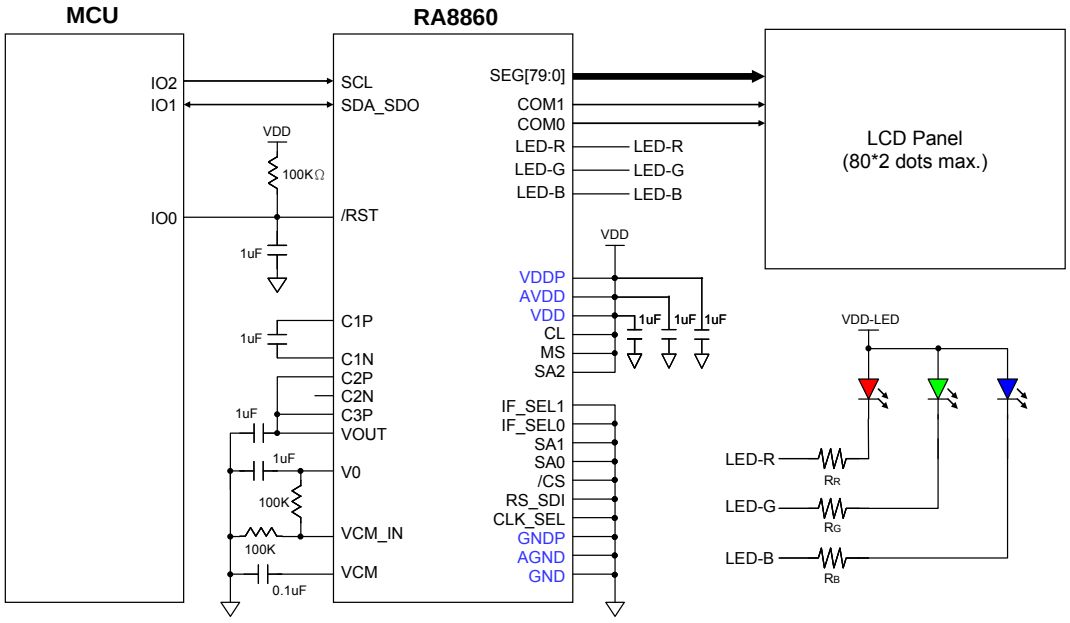


Figure 8-1 : Application Circuit – 1, VDD=3.3V, VOUT=2xVDD, I²C Mode

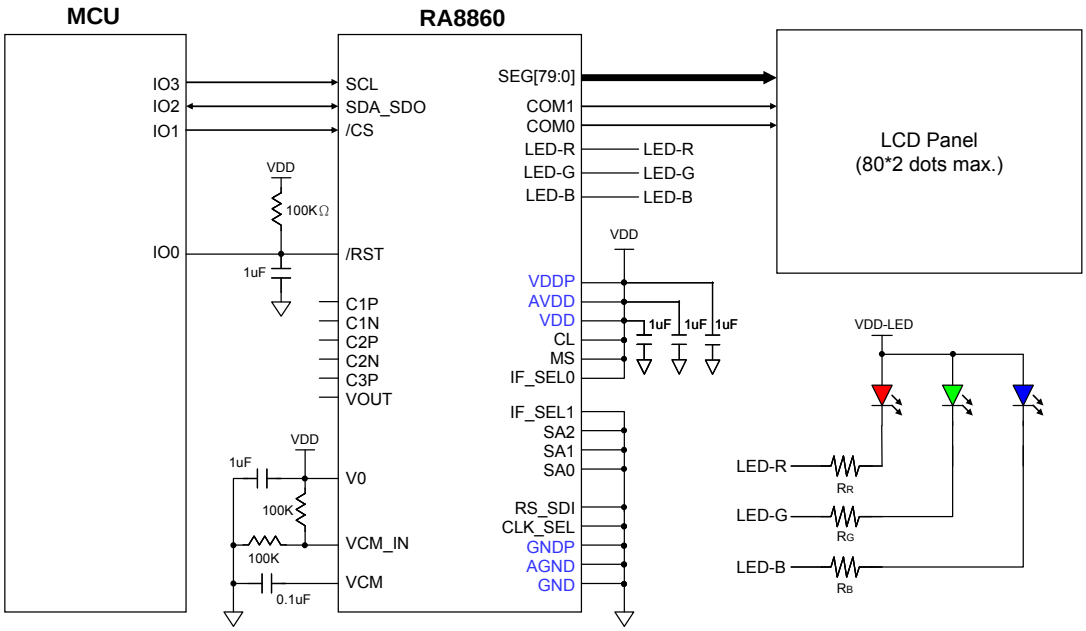


Figure 8-2 : Application Circuit – 2, VDD=5V Single Power, 3-wires SPI

Figure 8-3 is similar to Figure 8-1 but it's a cascade application of RA8860. Single 3.3V power and 2X Booster for VOUT, and LCD voltage (V0) is generated from master RA8860. Because it's an I^2C interface, so the "SCL" and "SDA" are connected together for each RA8860. But note that the device address "SA[2:0]" of both RA8860 have to connect to defferent level. In cascade mode, the Booster and Regulator of Slave RA8860 were disabled. The LCD voltage V0 and VCM of Slave are from Master RA8860. And signal "CL" is clock input which receives clock from Master's "CLK_OUT". Signal "SYNC" is input that receives synchronous signals from Master's "SYNC".

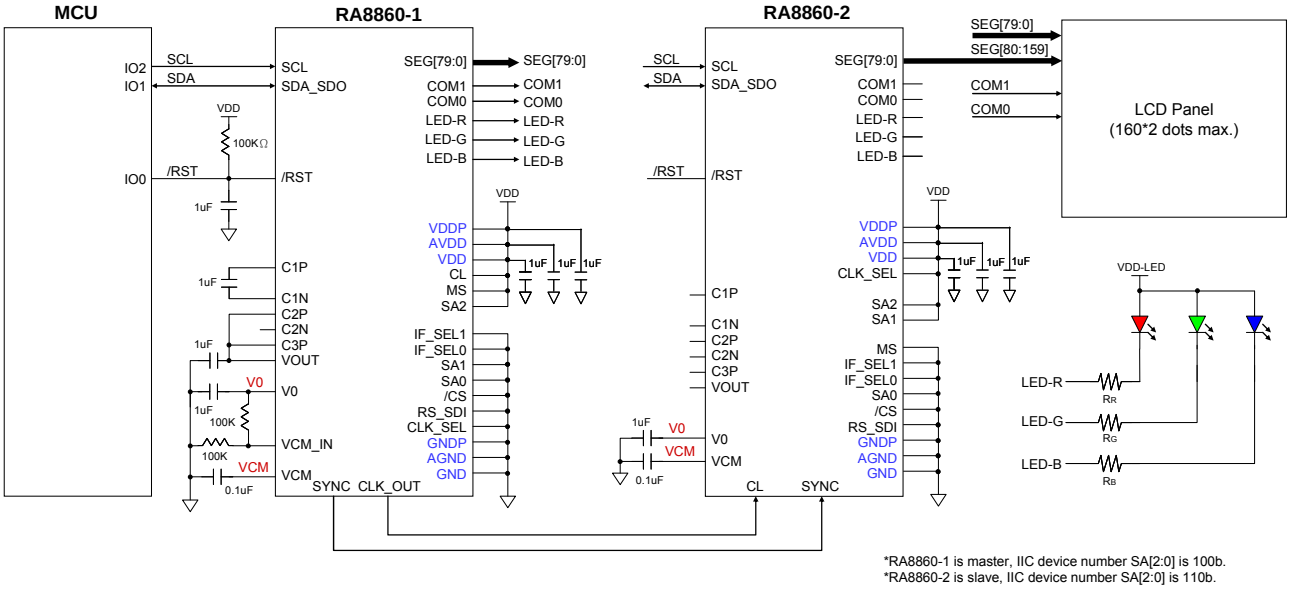


Figure 8-3 : Application Circuit – 3, VDD=3.3V , VOUT=2xVDD, I^2C Mode

9. Register Setting Sequence

9-1 Master Mode Initial Sequence

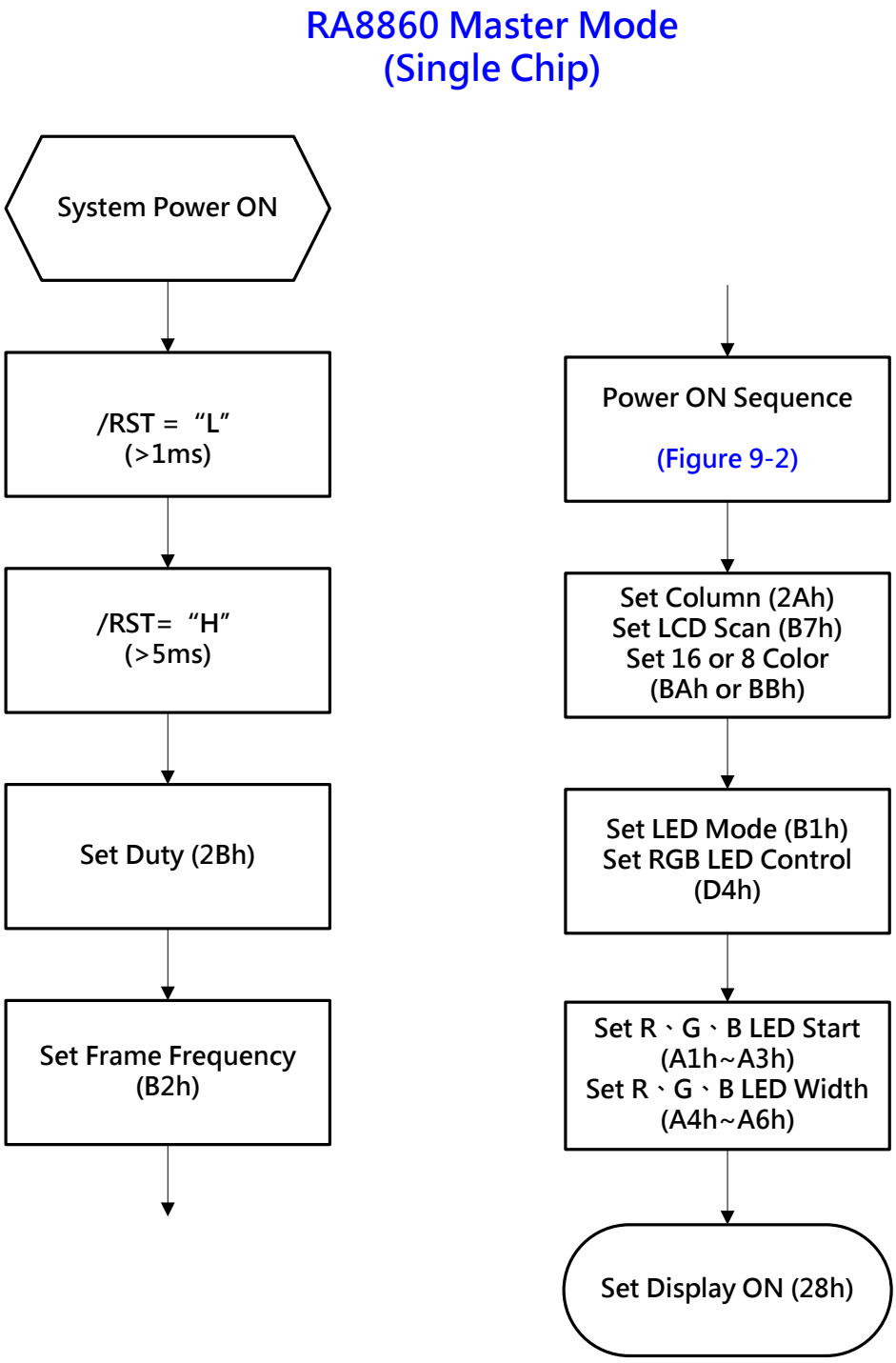


Figure 9-1 : Master Mode Initial Sequence

9-2 Power ON Sequence

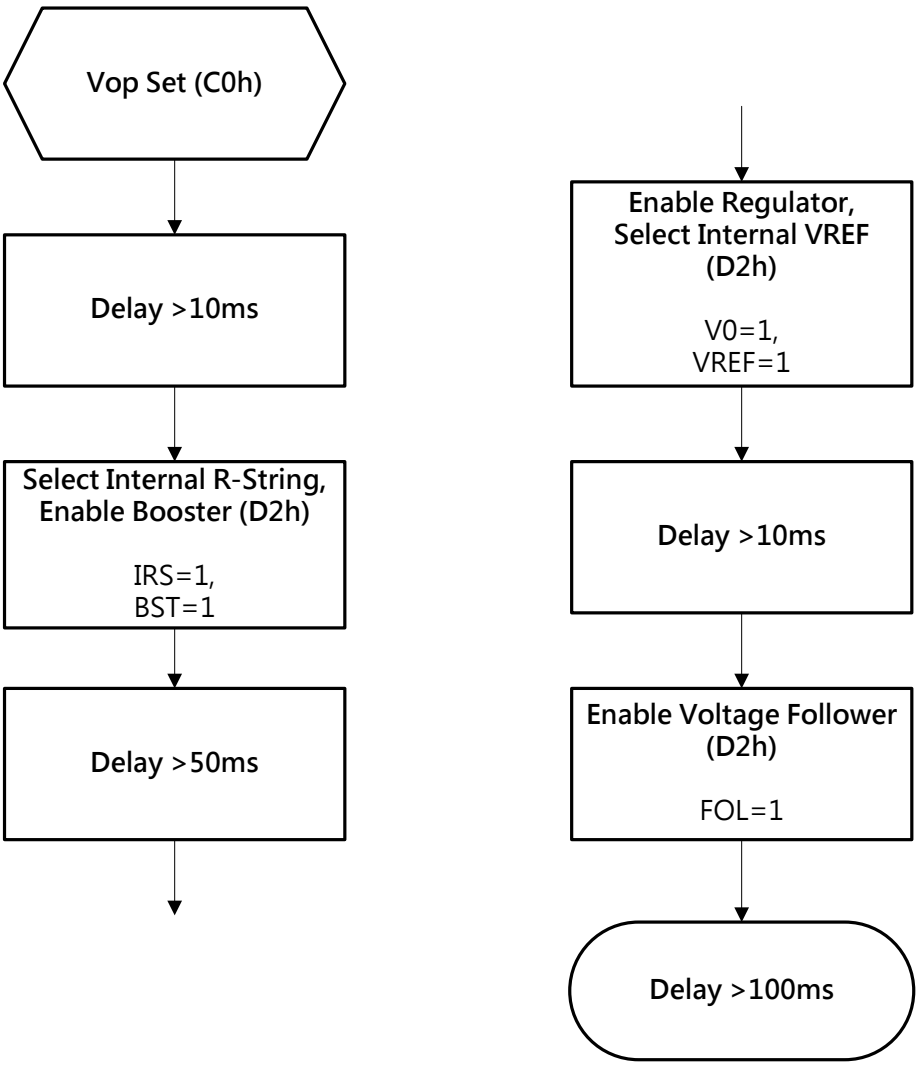


Figure 9-2 : Power ON Sequence

9-3 Sleep Mode and Wake Up Sequence

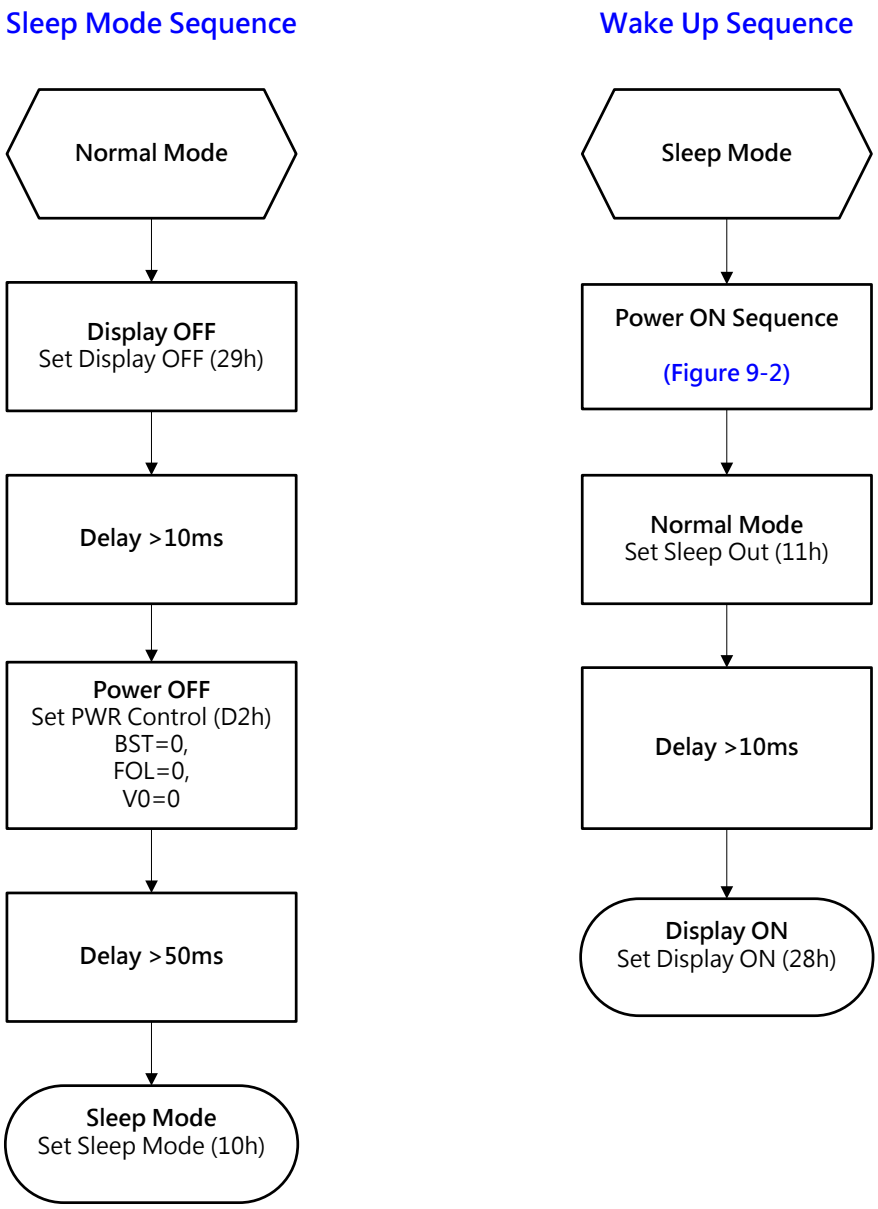


Figure 9-3 : Sleep Mode and Wake Up Sequence

9-4 Master Slave Mode (Cascade) Initial Sequence

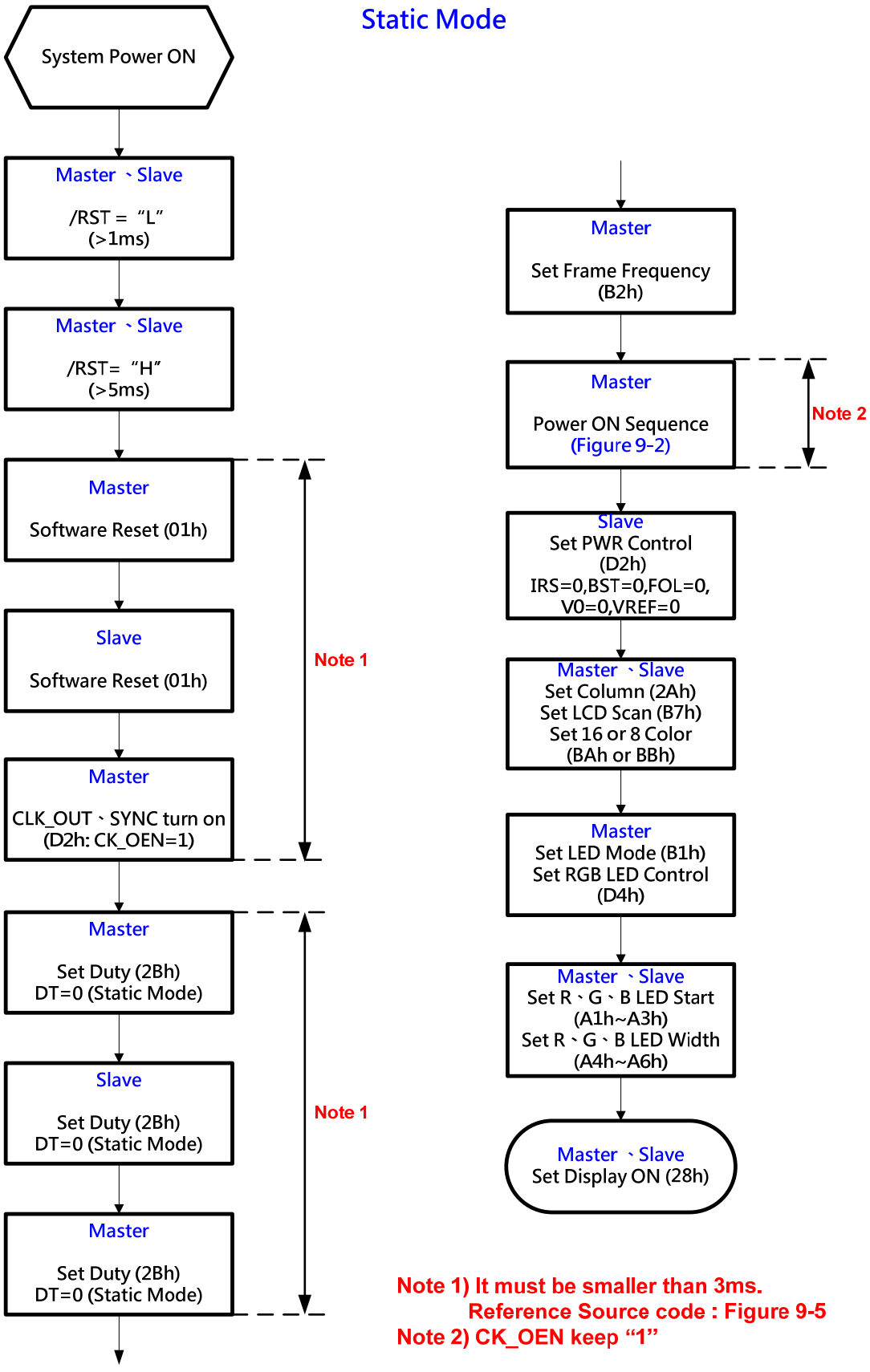
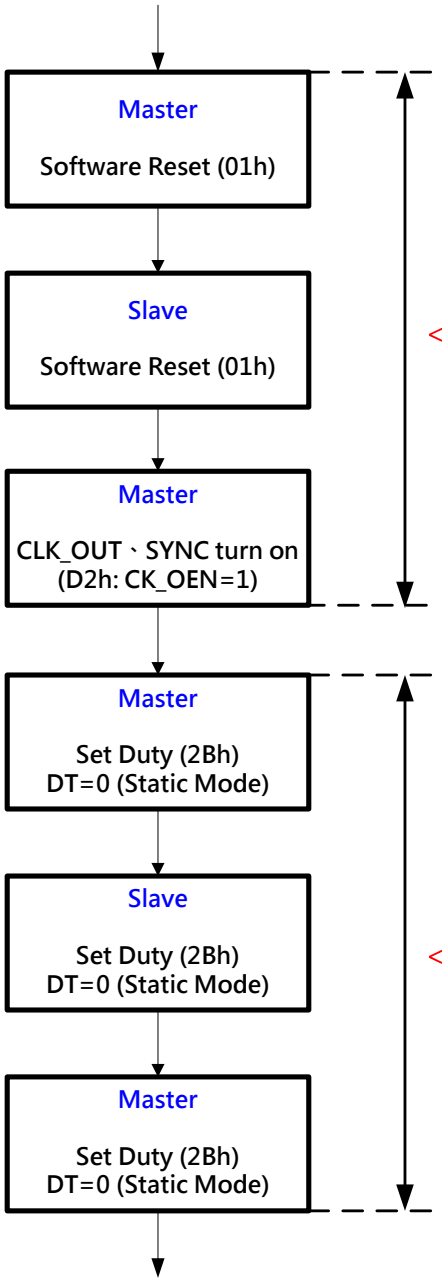


Figure 9-4 : Master Slave Mode Initial Sequence

9-5 Note 1) Reference Source Code




```
LCD_CmdWrite(0x01);              //Master: software reset
LCD_CmdWrite1(0x01);             //Slave: software reset
LCD_CmdWrite(0xD2);              //Set Reg D2h
LCD_DataWrite(0x20);             //CK_OEN=1
LCD_CmdWrite(0x2B);
LCD_DataWrite(0x00);             // Master Set Duty (Static)
LCD_CmdWrite1(0x2B);
LCD_DataWrite1(0x00);            // Slave Set Duty (Static)
LCD_CmdWrite(0x2B);
LCD_DataWrite(0x00);             // Master Set Duty (Static)
```

Figure 9-5 : Note 1) Reference Source Code

10. Demo Program

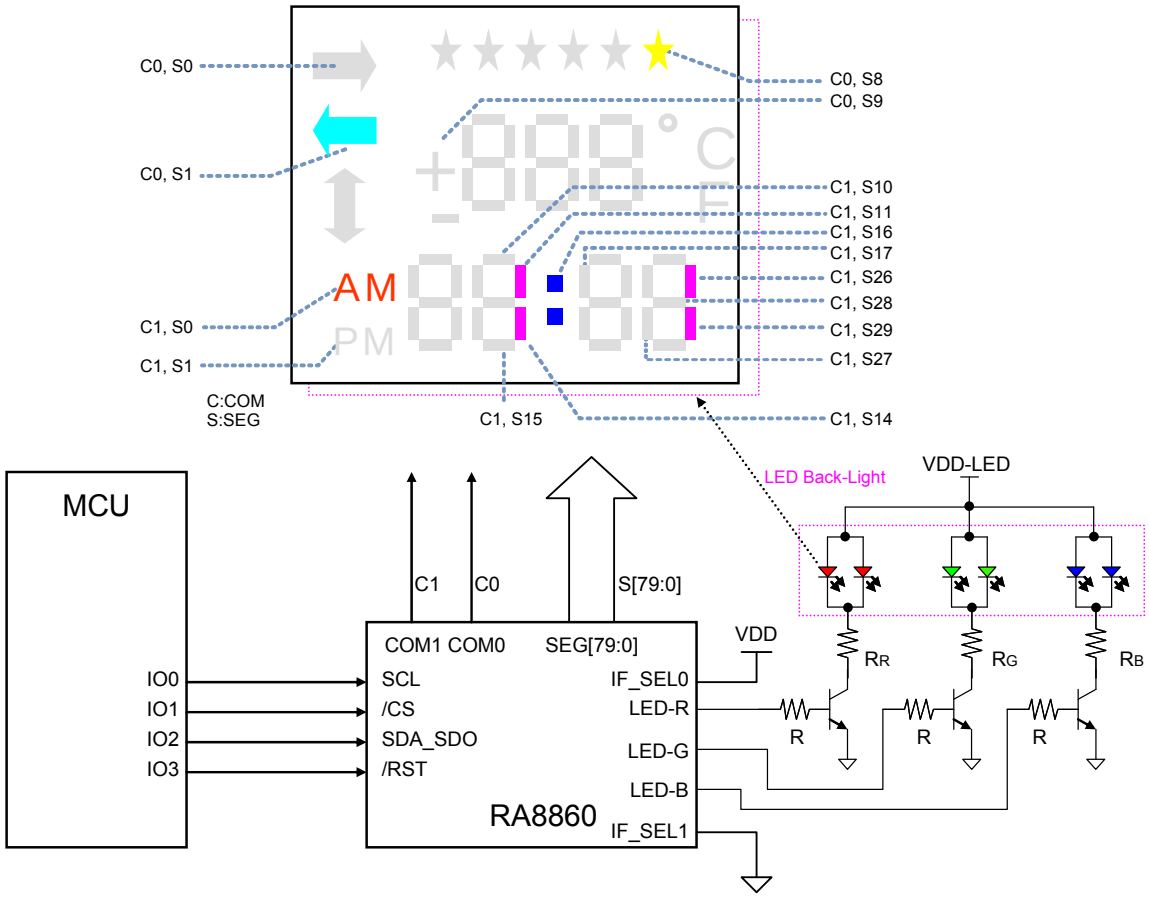


Figure 10-1 : Simple Application

Main Program:

```
//================== main process start ==================//
void main(void)
{
    unsigned char i;

    P0 = 0xff;
    P1 = 0xff;
    P2 = 0xff;
    P3 = 0xff;

    LCD_Reset();                // Reset RA8860
    LCD_Initial();              // Initial RA8860
    LCD_On();                   // Display on

    Address_Point(0x00);
    Memory_Write();
    for(i=0; i<=79; i++)
    {
        LCD_DataWrite(0x00);    // (C0, S0~S79) & (C1, S0~S79) : White
    }

    Address_Point(0x00);
    Memory_Write();
    LCD_DataWrite(0x90);        // (C0,S1): Aqua, (C0,S0): White

    Address_Point(0x04);
    Memory_Write();
    LCD_DataWrite(0x01);        // (C0,S9): White, (C0,S8): Yellow

    Address_Point(0x40);
    Memory_Write();
     LCD_DataWrite(0x03);       // (C1,S1): White, (C1,S0): Red

     Address_Point(0x45);
     Memory_Write();
     LCD_DataWrite(0x20);       // (C1,S11): Pink, (C1,S10): White

     Address_Point(0x47);
     Memory_Write();
     LCD_DataWrite(0x02);       // (C1,S15): White, (C1,S14): Pink

     Address_Point(0x48);
     Memory_Write();
     LCD_DataWrite(0x0E);       // (C1,S17): White, (C1,S16): Navy Blue

    Address_Point(0x4D);
    Memory_Write();
     LCD_DataWrite(0x02);       // (C1,S27): White, (C1,S26): Pink

     Address_Point(0x4E);
     Memory_Write();
     LCD_DataWrite(0x20);       // (C1,S29): Pink, (C1,S28): White

    Blink_Speed(0x04);          // Blinking Interval : ~850ms
    Blink_ Address(0x90);       // (C1,S16)
    Blink_On();                 // Blinking On

    while(1);
 }
```

```
// Related subroutine:
// ========== Hardware Reset ==========
void LCD_Reset(void)
{
    bRST = 0;
    Delay100ms(1);
    bRST = 1;
    Delay100ms(1);
}


// ========== 3 wire SPI Cycle ==========
void LCD_CmdWrite(unsigned char LCD_data)
{
//SPI initial
    LCD_ZCS = 1;
    LCD_SCK = 1;
    LCD_SDA = 1;
    LCD_ZCS = 0;

// A0= 0
    LCD_SCK = 0;
    LCD_SDA = 0;
    LCD_SCK = 1;
    Delay2us(1);

// RW = 0
    LCD_SCK = 0;
    LCD_SDA = 0;
    LCD_SCK = 1;
    LCD_SPI_SendData(LCD_data);
    LCD_ZCS = 1;
}


void LCD_DataWrite(unsigned char LCD_data)
{
//SPI initial
    LCD_ZCS = 1;
    LCD_SCK = 1;
    LCD_SDA = 1;
    LCD_ZCS = 0;

// A0 = 1
    LCD_SCK = 0;
    LCD_SDA = 1;
    Delay2us(2);
    LCD_SCK = 1;
    Delay2us(1);

// RW = 0
    LCD_SCK = 0;
    LCD_SDA = 0;
    Delay2us(2);
    LCD_SCK = 1;
    LCD_SPI_SendData(LCD_data);
    LCD_ZCS = 1;
}
```

```
unsigned char LCD_DataRead(void)
{
    unsigned char LCD_data;
//SPI initial
    LCD_ZCS = 1;
    LCD_SCK = 1;
    LCD_SDA = 1;
    LCD_ZCS = 0;

// A0 = 1
    LCD_SCK = 0;
    LCD_SDA = 1;
    LCD_SCK = 1;

// RW = 1
    LCD_SCK = 0;
    LCD_SDA = 1;
    LCD_SCK = 1;
    LCD_data = LCD_SPI_GetData();
    LCD_ZCS = 1;
}


void LCD_SPI_SendData(unsigned char buf)
{
    unsigned char i,SPI_Data;

    for(i=0 ; i<8 ; i++)
    {
        SPI_Data = buf & 0x80;
        LCD_SCK = 0;
        if(SPI_Data==0)
            LCD_SDA = 0;
        else
            LCD_SDA = 1;
     LCD_SCK = 1;
     buf <<= 1;
    }
    LCD_SCK = 1;
    LCD_SDA = 1;
}


unsigned char LCD_SPI_GetData(void)
{
    unsigned char i, buf;

    for(i=0 ; i<8 ; i++)
    {
        LCD_SCK = 0;
        buf <<= 1;
        LCD_SCK = 1;

        if(LCD_SDA)
        buf |= 0x01;
    }
    LCD_SCK = 1;
    LCD_SDA = 1;
    return buf;
}
```

```
// ========== RA8860 Initialization ==========
void LCD_Initial(void)
{
    LCD_CmdWrite(0x2B);
    LCD_DataWrite(0x01);      // Set Duty= 1/2 Duty

    LCD_CmdWrite(0xB2);
    LCD_DataWrite(0x01);      // Frame Frequency=75Hz
    Delay10ms(1);

//Power ON Sequence

    LCD_CmdWrite(0xC0);
    LCD_DataWrite(0x08);      // Vo=5V
    Delay10ms(1);

    LCD_CmdWrite(0xD2);
    LCD_DataWrite(0x18);      // Select Internal R-string, Enable Booster
    Delay10ms(5);

    LCD_CmdWrite(0xD2);
    LCD_DataWrite(0x1B);      // Enable Regulator, Select Internal VREF
    Delay10ms(1);

    LCD_CmdWrite(0xD2);
    LCD_DataWrite(0x1F);      // Enable Voltage Follower
    Delay10ms(10);

    LCD_CmdWrite(0x2A);
    LCD_DataWrite(0x27);      // Maximum Column = 27h = 39 (80/2 - 1)

    LCD_CmdWrite(0xBA);       // 16 color
                              // LCD_CmdWrite(0xBB);  //8 color

    LCD_CmdWrite(0xB1);
    LCD_DataWrite(0x01);      // LED high active
                              // LCD_DataWrite(0x00);  //LED low active

    LCD_CmdWrite(0xA1);
    LCD_DataWrite(6);         // Red LED Start Waveform Position Setting

    LCD_CmdWrite(0xA2);
    LCD_DataWrite(6);         //Green LED Start Waveform Position Setting

    LCD_CmdWrite(0xA3);
    LCD_DataWrite(6);         // Blue LED Start Waveform Position Setting

    LCD_CmdWrite(0xA4);
    LCD_DataWrite(250);       // Red LED Width Waveform Setting

    LCD_CmdWrite(0xA5);
    LCD_DataWrite(250);       // Green LED Width Waveform Setting

    LCD_CmdWrite(0xA6);
    LCD_DataWrite(250);       // Blue LED Width Waveform Setting
}
```

```
// ========== Subroutine for Display On ==========
void LCD_On(void)
{
    LCD_CmdWrite(0x28);
}

// ========== Subroutine for Address Point ==========
void Address_Point(unsigned char Data)
{
    LCD_CmdWrite(0x2F);
    LCD_DataWrite(Data);
}

// ========== Subroutine for Memory Write ==========
void Memory_Write(void)
{
    LCD_CmdWrite(0x2C);
}

// ========== Subroutine for Blinking Interval ==========
void Blink_Speed(unsigned char Data)
{
    LCD_CmdWrite(0x26);
    LCD_DataWrite(Data);
}

// ========== Subroutine for Blinking Address ==========
void Blink_Address(unsigned char Data)
{
    LCD_CmdWrite(0x25);
    LCD_DataWrite(Data);
}

// ========== Subroutine for Blinking Enable ==========
void Blink_On(void)
{
    LCD_CmdWrite(0x24);
    LCD_DataWrite(0x01);
}
```